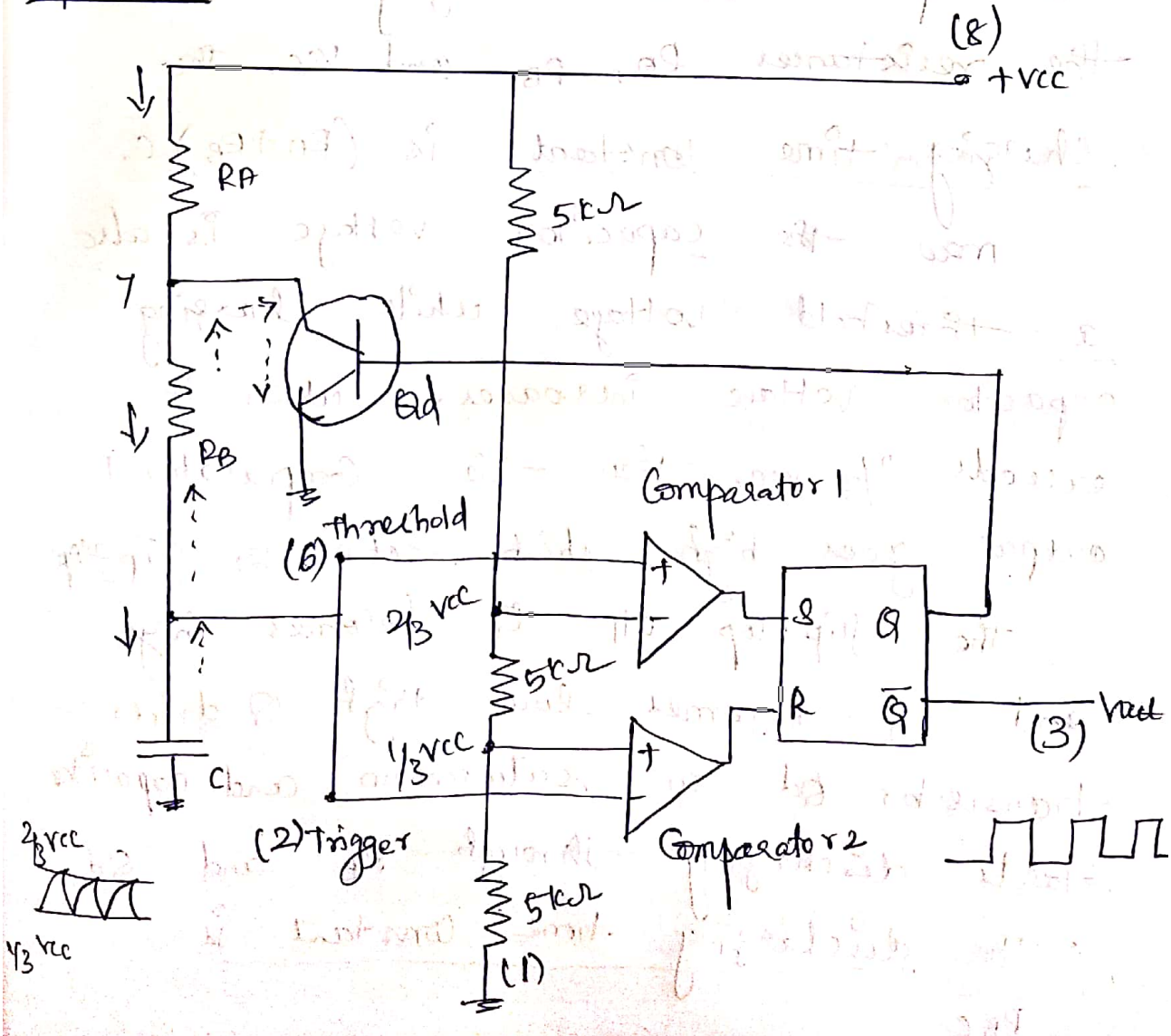
Astable Multivibrator using IC555:

This circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running non-sinusoidal oscillator.

The threshold input is connected to the trigger input. Two external resistances R_A, R_B and capacitor C is used in the circuit.

Operation:



When the flipflop is set, Q is high which drives the transistor Qd in saturation and capacitor gets discharged. now the capacitor voltage is trigger voltage.

so while discharging, when it becomes less than 1/3 Vcc, Comparator 2 o/p goes high. this resets the flipflop hence Q goes low and $\bar{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and Vcc. The charging time constant is $(R_A + R_B)C$.

now the capacitor voltage is also a threshold voltage. while charging capacitor voltage increases. when it exceeds 2/3 Vcc, then the Comparator 1 output goes high which sets the flipflop.

The flipflop o/p Q becomes high and $\bar{Q}$ becomes low. high Q drives transistor Qd in saturation and capacitor starts discharging through R_B and Qd.

∴ The discharging time constant is $R_B C$

when capacitor voltage becomes less than $1/3$ Vcc, comparator 2 output goes high resetting the flipflop. this cycle repeats.

Q high → $\bar{Q}$ low → transistor Qd on ⇒ short circuit

Capacitor discharges.

capacitor voltage $< 1/3$ Vcc ⇒ comp2 o/p high (trigger voltage)

→ Reset → Q low → $\bar{Q}$ high.

↓

Qd OFF ⇒ open circuit.

Capacitor charges.

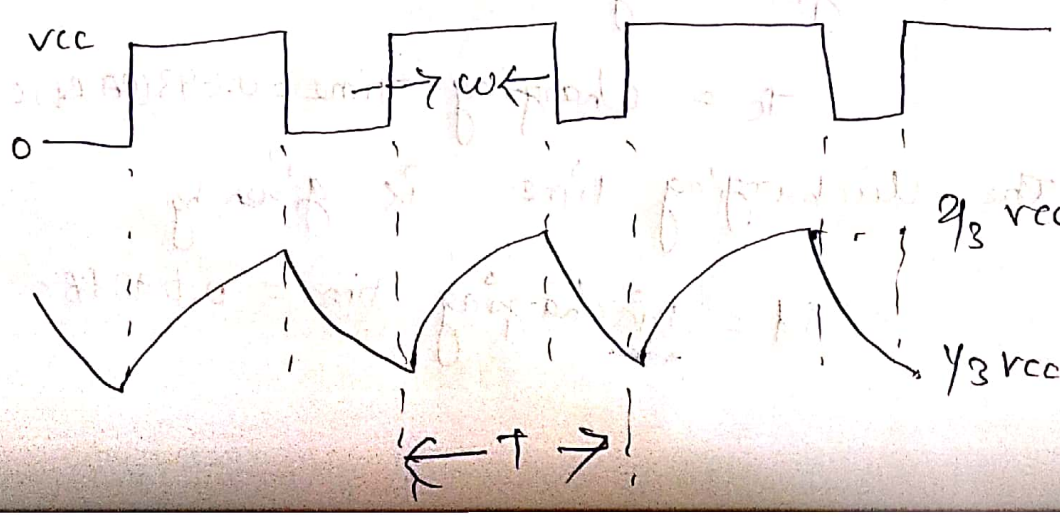
capacitor voltage $> 2/3$ Vcc ⇒ comp1 o/p high. (threshold voltage)

→ set → Q high → $\bar{Q}$ low

↓

Qd on ⇒ short circuit

Capacitor discharges



Duty cycle :-

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric.

The ratio of high output period and low output period is given by a parameter called duty cycle.

w = time for o/p is high.

T = time of one cycle.

Duty cycle is defined as the ratio of or time (i.e) high o/p to the total time of one cycle.

$$D = \text{duty cycle} = \frac{w}{T}$$

$$\%\ D = \frac{w}{T} \times 100\ \%$$

The charging time for the capacitor is given by

T_c = charging time = $0.693(R_A + R_B)C$

The discharging time is given by

T_d = Discharging time = $0.693 R_B C$

$\therefore \quad T = T_c + T_d$

$= 0.693 (R_A + R_B) C + 0.693 R_B C$

$= 0.693 (R_A + 2R_B) C$

$W = T_c = 0.693 (R_A + R_B) C$

$\% D = \frac{W}{T} = \frac{0.693 (R_A + R_B) C}{0.693 (R_A + 2R_B) C}$

$$\boxed{\% D = \frac{R_A + R_B}{R_A + 2R_B} \times 100}$$

The frequency of oscillation is given by

$$f = \frac{1}{T} = \frac{1}{0.693 (R_A + 2R_B) C}$$

$$\boxed{f = \frac{1.44}{(R_A + 2R_B) C}}$$

if R_A is smaller than R_B, duty cycle approaches to 50 % and o/p waveform approaches to square wave.

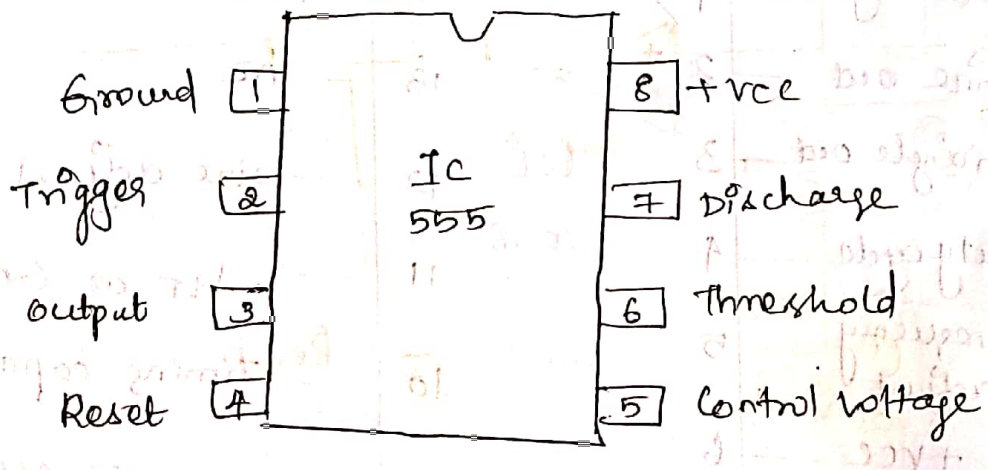
5.12. Timer IC555.

The timer IC555 is most versatile linear integrated device introduced by signetics corporation in early 1970.

The Ic 555 timer combines the following elements

1) A relaxation oscillator
2) R-S flipflop
3) Two comparators
4) Discharge transistor.

5.12.1 pin and functional block diagram of IC555.



pin diagram.

This is 8 pin Ic times.

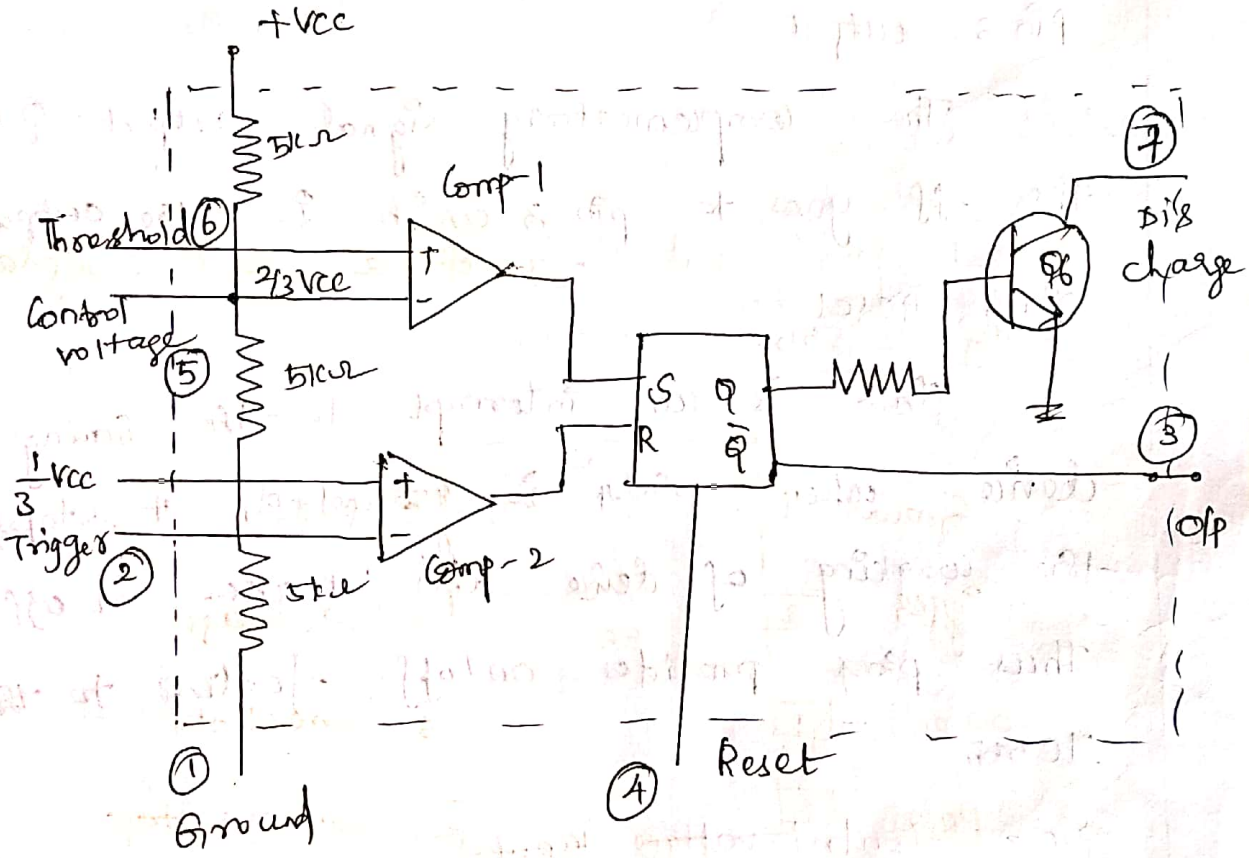
The functional block diagram is explained through the discussion of various pins.

Pin 1 : Ground

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger

The IC555 uses two comparators. The voltage divider consists of three equal resistances.



Block diagram of IC555 timer

Due to voltage divider, the voltage of non inverting terminal of comparator 2 is fixed at $\frac{Vcc}{3}$.

The inverting input of comparator is compared with $\frac{Vcc}{3}$ is nothing but trigger

input brought out as pin number 2.

When the trigger input is slightly less than $\frac{V_{cc}}{3}$, the comparator 2 output goes high. This o/p is given to reset input of R-S flip flop.

So high output of comparator 2 resets the flipflop.

pin 3: output :-

The complementary signal output $\bar{Q}$ of the ff goes to pin 3 which is the output.

pin 4 Reset :-

This is an interrupt to the timing device. When pin 4 is grounded, it stops the working of device and makes it off. Thus pin 4 provides on/off feature to the IC 555.

pin 5: Control voltage input :-

In most of the applications, external control voltage input is not used.

This pin is nothing but the inverting input terminal of comparator 1. The voltage divider holds the voltage of this input at 2/3 V_{cc}.

This is reference level for comparator 1 with which threshold is compared.

If reference level required is other than 2/3 Vcc for comparator 1 then external input is to be given to pin 5.

If external i/p applied to pin 5 is alternating then the reference level for comparator 1 keeps on changing above and below 2/3 Vcc.

Due to this, the variable pulse width output is possible. This is called pulse width modulation, which is possible due to pin 5.

pin 6 : Threshold :-

This is the non inverting input terminal of comparator. The external voltage is applied to this pin 6.

When this voltage is more than 2/3 Vcc, the comparator 1 output goes high. This is given to the set i/p of RS ff. Thus high o/p of comparator 1 sets the flip flop. This makes Q of flip flop high & $\bar{Q}$ low. Thus the o/p of IC555 at pin 3 goes low.

In short

For threshold $> \frac{2}{3}$ Vcc, flipflop → set

Q → high → o/p at pin 3 → low.

For trigger $< \frac{1}{3}$ Vcc, flipflop → reset

Q → low → o/p at pin 3 → high.

pin 7 : Discharge :

This pin is connected to the collector of the discharge transistor Qd.

When Q is low, transistor Qd is off. It acts as an open circuit to the external capacitor C to be connected across it, so capacitor C can charge.

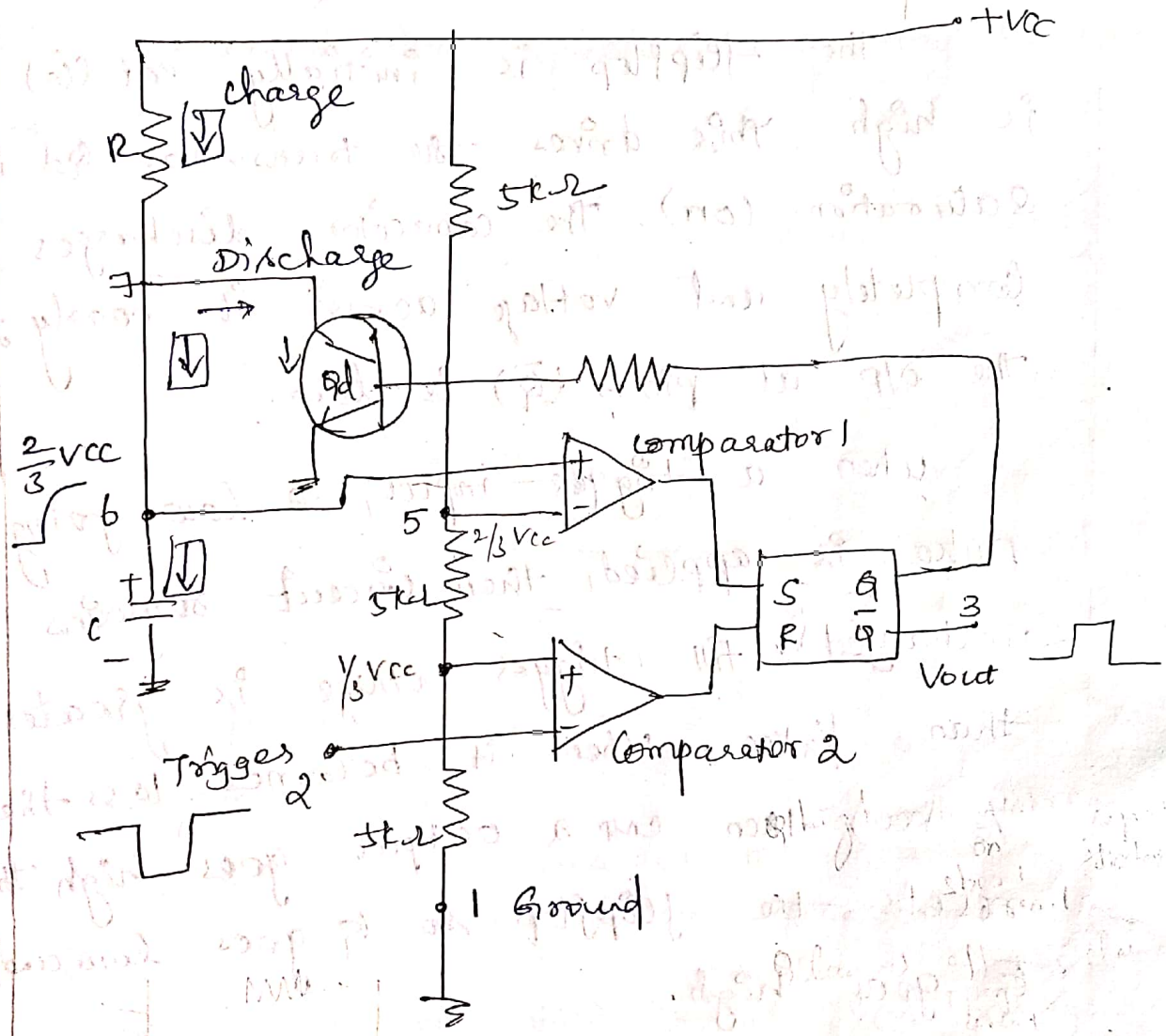
When Q is high which drives the base of Qd high, driving transistor Qd in saturation, It acts as short circuit shorting the external capacitor, C to be connected across it.

pin 8 : Supply +Vcc.

The Ic555 timer can work with any supply voltage between +5V to 16V.

5.6.2 Monostable multivibrator using IC555:

The Ic 555 timer can be operated as a monostable multivibrator by connecting an external resistor and a capacitor.



monostable operation of IC555

The circuit has only one stable state. when trigger is applied, it produces a pulse at the o/p and returns back to its stable state.

The duration of the pulse depends on

the values of R and C.

It has only one stable state, it is called one shot multivibrator.

Operation:

The flipflop is initially set (ie) Q is high. This drives the transistor Qd in saturation. (on). The capacitor discharges completely and voltage across it nearly zero. The o/p at pin 3 ($\bar{Q}$) is low.

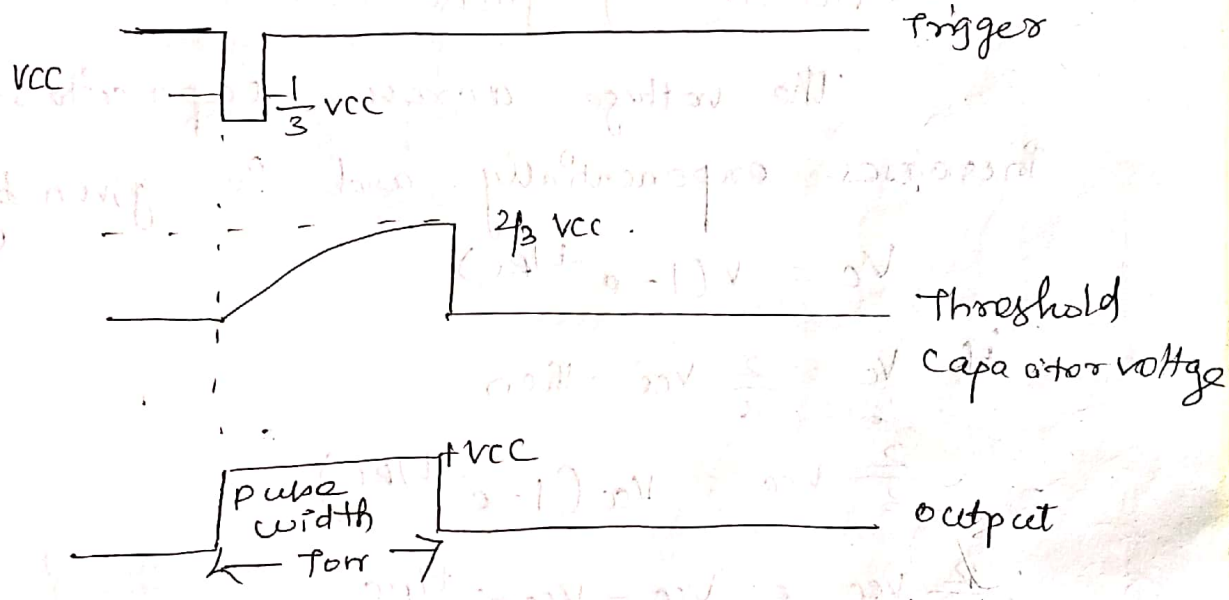
When a trigger input, a low going pulse is applied, then circuit remains unchanged till trigger voltage is greater than 1/3 Vcc. When it becomes less than 1/3 Vcc, then CMP 2 output goes high. This resets the flipflop so Q goes low and $\bar{Q}$ goes high.

Low Q makes the transistor Q off. Hence capacitor starts charging through resistor R.

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6.

When this voltage becomes more than 2/3 Vcc, then comparator 1 output goes high. This sets the ff (i.e) Q becomes high and $\bar{Q}$ low.

This high Q drives the transistor Qd in saturation. the capacitor C quickly discharges through Qd.



waveforms of monostable operation.

So it can be noted that Vout at pin 3 is low at start, when trigger is less than 1/3 Vcc it becomes high and when threshold is greater than 2/3 Vcc again becomes low, till next trigger pulse occurs.

Initially o/p is low —
Trigger is < 1/3 Vcc o/p high

Threshold > $\frac{2}{3}V_{cc}$ O/P low.

The pulse width of this rectangular pulse is controlled by the charging time of capacitor.

This depends on the time constant RC. The RC controls the pulse width.

Derivation of pulse width:-

The voltage across capacitor increases exponentially and is given by

$$V_c = V(1-e^{-t/RC})$$

if $V_c = \frac{2}{3}V_{cc}$ then

$$\frac{2}{3}V_{cc} = V_{cc}(1-e^{-t/RC})$$

$$\frac{2}{3}V_{cc} = V_{cc} - V_{cc}e^{-t/RC}$$

$$\frac{2}{3}V_{cc} - V_{cc} = -V_{cc}e^{-t/RC}$$

$$\frac{2}{3} - 1 = -e^{-t/RC}$$

$$-1/3 = -e^{-t/RC}$$

$$e^{-t/RC} = 1/3$$

$$-t/RC = \ln 1/3$$

$$-t/RC = -1.0986$$

$$t = 1.0986RC \Rightarrow \boxed{t = 1.1RC}$$

The pulse width denoted as w is given by

$$W = 1.1RC$$

Applications of monostable multivibrator:

1) Frequency divider
2) Pulse width modulation
3) Linear Ramp Generator
4) Missing pulse detector
5) Pulse position modulation

Introduction

A phase locked loop is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. It is commonly abbreviated as PLL.

The PLL was first introduced in its discrete form in early 1930s. The high cost of realizing PLL in discrete form limited its use earlier.

Now with the advanced IC technology, PLLs are available as inexpensive monolithics ICs.

They are used in applications such as frequency synthesis, frequency modulation / demodulation, AM detection, tracking filters, FSK demodulator, tone detector etc.

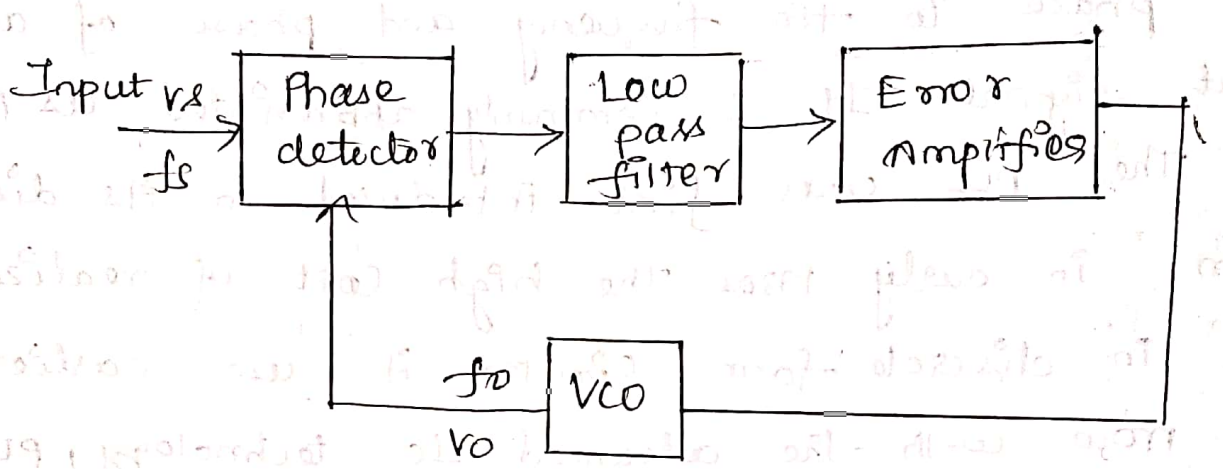
In this chapter we are going to discuss basic operating principle, popular PLL IC 565, and important applications of PLL.

3.2 Basic principles:

The basic block schematic of the PLL is shown in figure. The feedback system consists of

1) phase detector / comparator

2) A low pass filter
3) An error amplifier
4) A voltage controlled oscillator (VCO).



Block diagram of PLL

The phase detector compares the input frequency fs with feedback frequency fo and generates an output signal which is a function of the difference between the phases of the two input signals.

The output signal of the phase detector is a d.c voltage. the output of phase detector is applied to low pass filter to remove high frequency noise from the d.c voltage.

the output of low pass filter without high frequency noise is often referred to as error voltage or control voltage for VCO.

When control voltage is zero, VCO is in free running mode and its output frequency is called as center frequency f_o.

The non zero control voltage results in a shift in the VCO frequency from its free running frequency f_o to a frequency f given by

$$f = f_o + K_V V_c$$

Where K_V is the voltage to frequency transfer coefficient of the VCO. The error or control voltage applied as an input to the VCO, forces the VCO to changes its output frequency in the direction that reduces the difference between the input frequency and the output frequency of VCO.

This action commonly known as capturing, continues till the O/P frequency of VCO is same as the input signal frequency. Once the two frequencies are same, the circuit is said to be locked.

In locked condition, phase detector generates a constant dc level which is required to shift the output frequency of VCO

from centre frequency to the input frequency. once locked, (PLL tracks the frequency changes of the input signal.

Thus a PLL goes through three states

1) Free running
2) capture
3) phase lock.

3.3 Important Definitions Related to PLL.

Lock Range :-

When PLL is in lock, it can track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called lock range or tracking range of the PLL.

Capture range :-

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.

pull in time :-

The total time taken by the PLL to establish a lock is called pull in time.

This depends on the initial phase and frequency difference between the two signals as well as on the overall gain and the bandwidth of the low pass filter.

3.8 Monolithic phase locked loop IC 565.

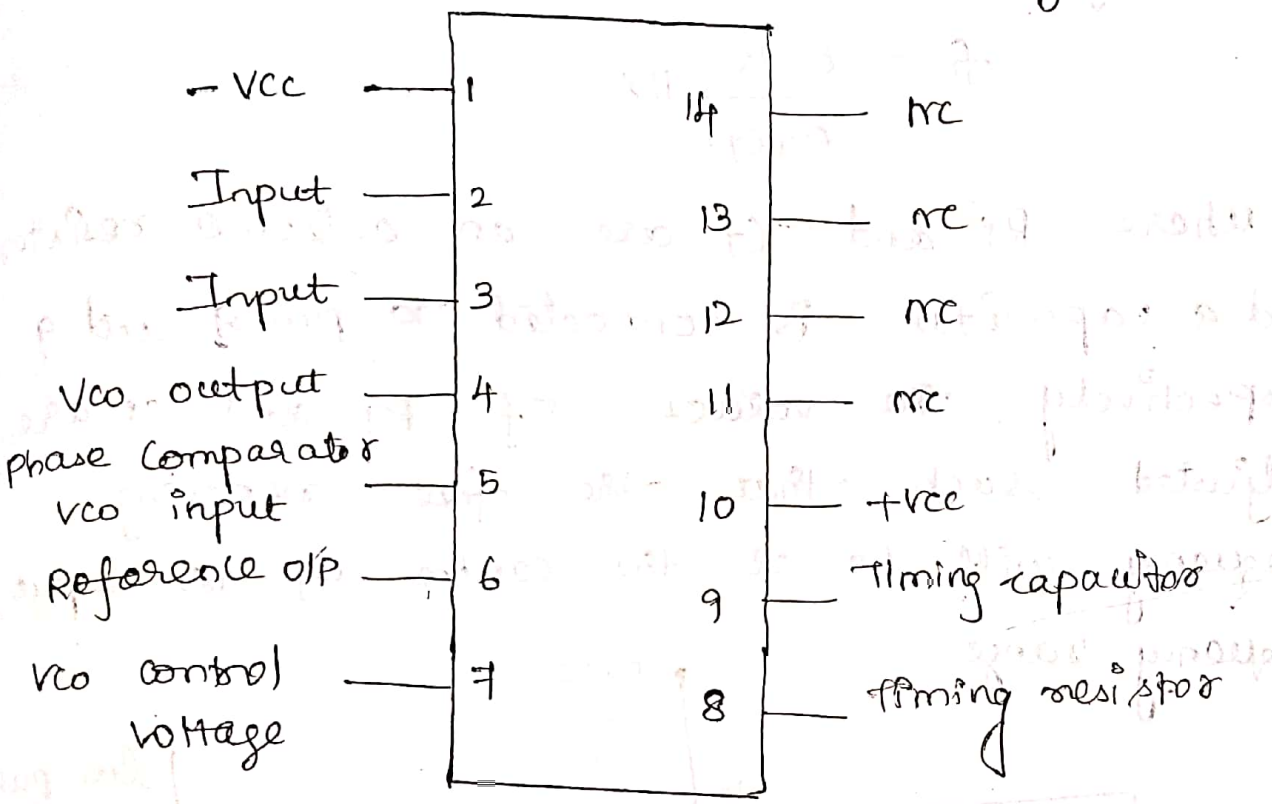
Monolithic PLLs are introduced by Signetics as SE/NE 560 series and by national Semiconductor as LM 560 series.

The SE/NE 560 series includes SE/NE 560, 561, 562, 564, 565 and 567. These ICs are differ mainly in operating frequency range, power supply requirements and frequency and bandwidth adjustment ranges.

3.8.1 IC 565:

IC 565 is available in a 14 pin DIP package and 10 pin metal can package.

Dual in line package



Pin configuration of IC565

The block diagram of IC 565 PLL consists of phase detector, amplifier, low pass filter and vco.

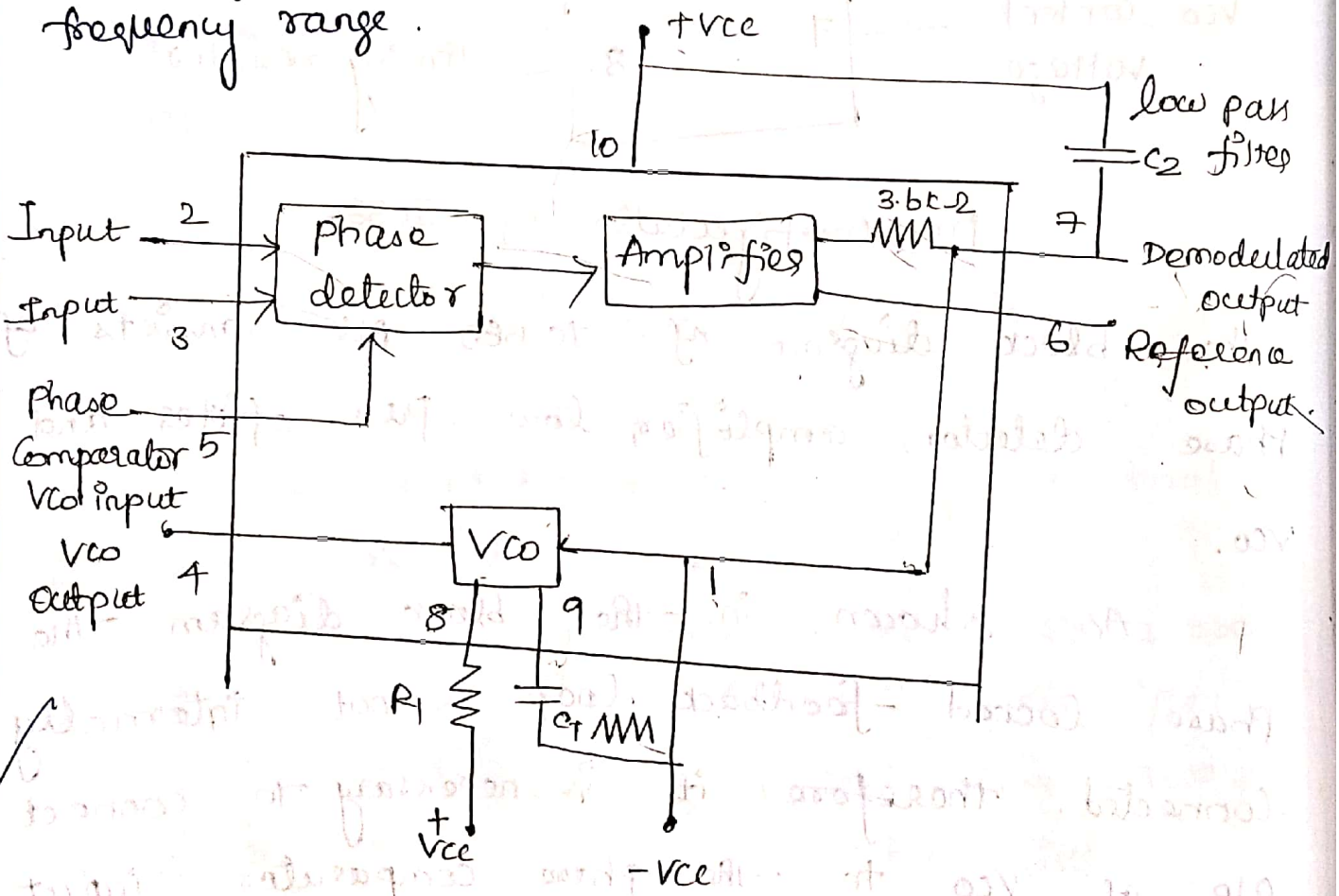
As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore it is necessary to connect o/p of vco to the phase comparator input externally.

The centre frequency of the PLL is determined by the free running frequency of the vco and it

is given as

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz}.$$

Where R_T and C_T are an external resistor and a capacitor is connected to pin 8 and 9 respectively. The values of R_T and C_T are adjusted such that the free running frequency will be at the centre of the input frequency range.



Block diagram of IC565 PLL

The value of R_T is restricted from 2kΩ to 20kΩ, but a capacitor can have any value.

A capacitor C2 connected between pin 7 and the positive supply it forms a loco pass filter with a internal resistance of 3.6 KΩ.

The value of filter capacitor C2 should be large enough to eliminate possible oscillations in the VCO voltage.

The lock range and capture range for IC565 PLL are given by the following equations.

$$f_L = \frac{\pm 8 f_o}{V} \text{ Hz}$$

f_o = free running frequency of VCO in Hz.

$$V = +V_{CC} + - (-V_{CC}) \text{ volts}$$

$$f_c = \pm \left[\frac{f_L}{2\pi (3.6)(10^3) C_2} \right]^{1/2}$$

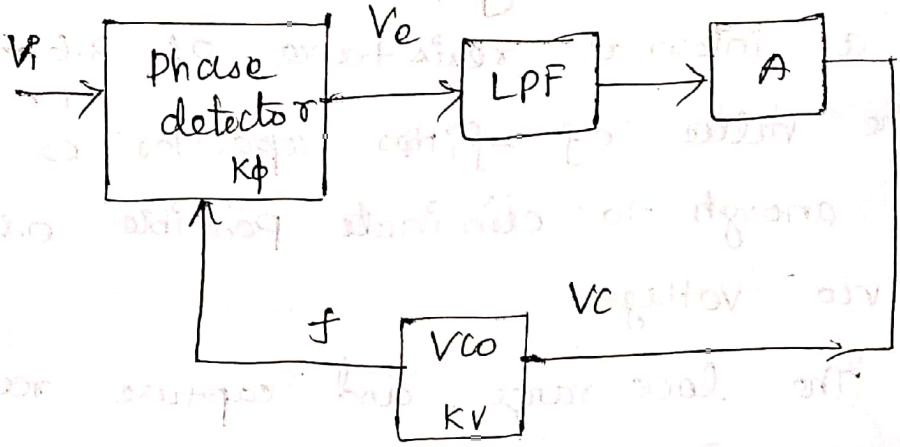
Lock range decreases with an increase in supply voltage.

3.8.1 Derivation of lock range:

If ϕ radians is the phase difference between the signal and the VCO voltage then the O/P voltage of the analog phase detector is given by

30

$$V_e = K_\phi (\theta_e - \pi/2)$$



Block diagram to determine lock range.

The output voltage of the phase detector is filtered by the low pass filter to remove the high frequency components.

The output of the filter is amplified by a gain A and then applied as the control voltage V_c to the VCO is given by

$$V_c = AV_e = K_\phi A (\theta_e - \pi/2). \quad \text{—①}$$

This control voltage V_c will result in a shift in the VCO frequency from its center frequency f_0 to a frequency f_i given by

$$f = f_0 + K_V V_c. \quad \text{—②}$$

when the PLL is locked into the input signal frequency f_i, we have

$$f = f_i = f_o + K_V V_c$$

Substitute the value of V_c in the above equation

$$f = f_i = f_o + K_V K_\phi A (\phi - \pi/2) \quad \text{---} (3)$$

$$f_i - f_o = K_V K_\phi A (\phi - \pi/2)$$

$$\phi - \pi/2 = \frac{f_i - f_o}{K_V K_\phi A}$$

$$\phi = \pi/2 + \frac{f_i - f_o}{K_V K_\phi A}$$

The maximum o/p voltage available from the phase detector occurs for $\phi = \pi$ and $\phi = 0$ radian is

$$V_c(max) = \pm K_\phi (\pi/2)$$

The corresponding value of the maximum control voltage available to drive the VCO will be

$$V_c(max) = \pm K_\phi (\pi/2) A.$$

Substitute the maximum value of V_c in eqn (3) we have

$$V_c(max) = \pm K_\phi (\pi/2) A$$

$$f = f_i = f_o + K_V K_\phi A (\pi/2)$$

$$= f_o \pm \Delta f_L.$$

where $\Delta f_L = \pm K_V K_\phi (\pi/2) A$.

$$2\Delta f_L = K_V K_\phi \pi A.$$

For IC 565 (PLL)

$$K_V = \frac{\delta f_o}{V}$$

$$V = \pm V_{cc} - (V_{cc})$$

$$K_\phi = \frac{1.4}{\pi} \qquad A = 1.4.$$

Hence the lock in range in

$$\Delta f_L = \frac{\delta f_o}{V} \times \frac{1.4}{\pi} \times \frac{\pi}{2} \times 1.4$$

$$\boxed{\Delta f_L = \pm \frac{0.84 f_o}{V}}$$

3.8.2 Derivation of capture range :-

Initially when PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. the phase angle difference between the signal and the VCO output voltage will be

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o) t + \Delta\theta$$

the phase angle difference will change with time

at a rate is given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi (\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta f$

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)}$$

$f_1 = \frac{1}{2\pi RC}$. In the slope portion of LPF

$(f/f_1)^2 \gg 1$

$$\therefore \quad T(f) = \frac{f_1}{jf}$$

The fundamental input frequency term supplied to the low pass filter by a phase detector will be at the difference frequency $\Delta f = f_s - f_o$

If $\Delta f > 3f_1$, the LPF transfer function will be

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{f_s - f_o}$$

The voltage V_c to drive the VCO is

$$V_c = V_e \times T(f) \times A$$

$$V_{c(max)} = V_{e(max)} \times T(f) \times A$$

$$= \pm K_\phi (\pi/2) A \times (f_1/\Delta f)$$

The corresponding value of the maximum frequency shift will be given by

$$(f - f_0)_{max} = K_V V_{c(max)}$$

$$= \pm K_V K_\phi (\pi/2) A \times (f_1/\Delta f)$$

For the acquisition of the signal frequency f_s, we must have that $f_s = f$. So that the maximum signal frequency range can be required by the PLL will be

$$(f_s - f_0)_{max} = \pm K_V K_\phi (\pi/2) A (f_1/\Delta f_{cap})$$

Since $\Delta f_{cap} = (f_s - f_0)_{max}$.

$$(\Delta f_{cap})^2 = K_V K_\phi (\pi/2) A f_1$$

Since $\Delta f_L = \pm K_V K_\phi (\pi/2) A$

$$(\Delta f_{cap})^2 = f_1 \Delta f_L.$$

$$\Delta f_{cap} = \pm \sqrt{f_1 \Delta f_L}$$

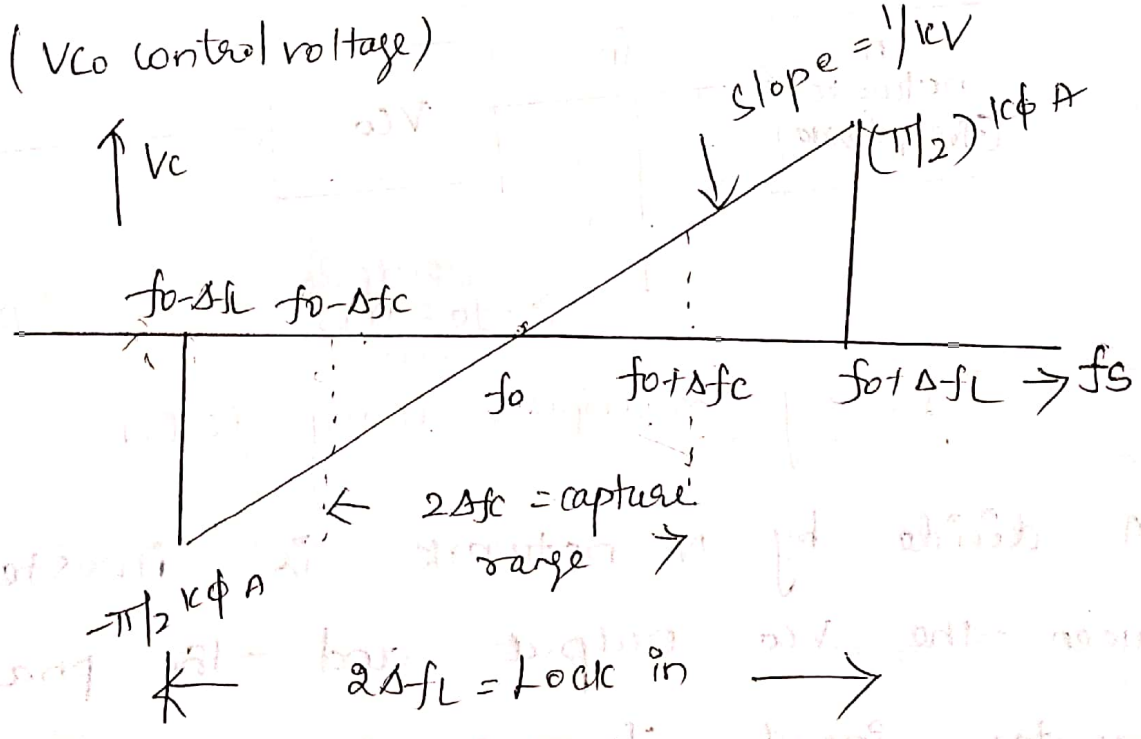
$$= \pm \sqrt{f_1 \Delta f_L}$$

$$= \pm \left[\frac{\Delta f_L}{2\pi RC}\right]^{1/2}$$

For IC PLL 565, $R = 3.6\,k\Omega$

$$\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C}\right]^{1/2}$$

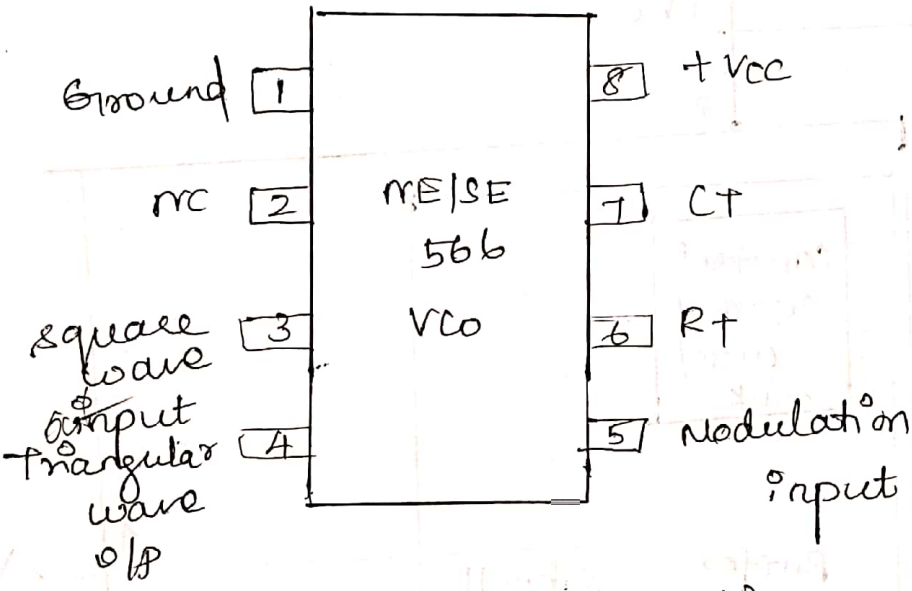
The total capture range is $2\Delta f_{cap}$.



PLL lock in range & capture range.

3.7 Voltage Controlled oscillator (VCO) NE/SE 566 VCO:

A common type of VCO available in IC form is signetics NE/SE 566. The pin diagram and block diagram of 566 VCO are shown in figure.

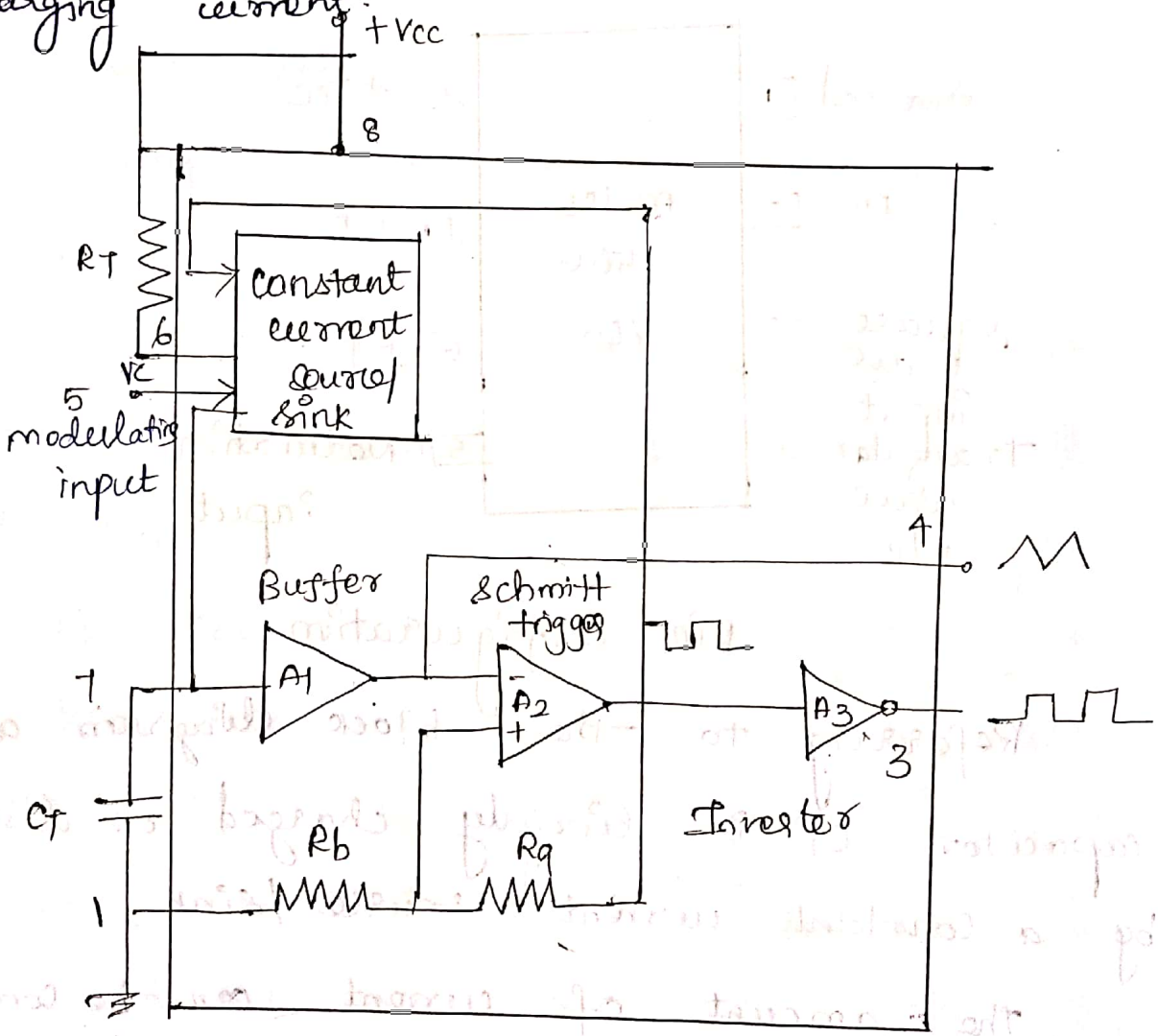


Pin configuration.

Referring to the block diagram a timing capacitor C1 is linearly charged or discharged by a constant current source/sink.

The amount of current can be controlled by changing the voltage Vc applied at the modulating input or by changing the timing resistor R1 external to IC chip.

The voltage at pin 5 is held at the same voltage as pin 5. Thus if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

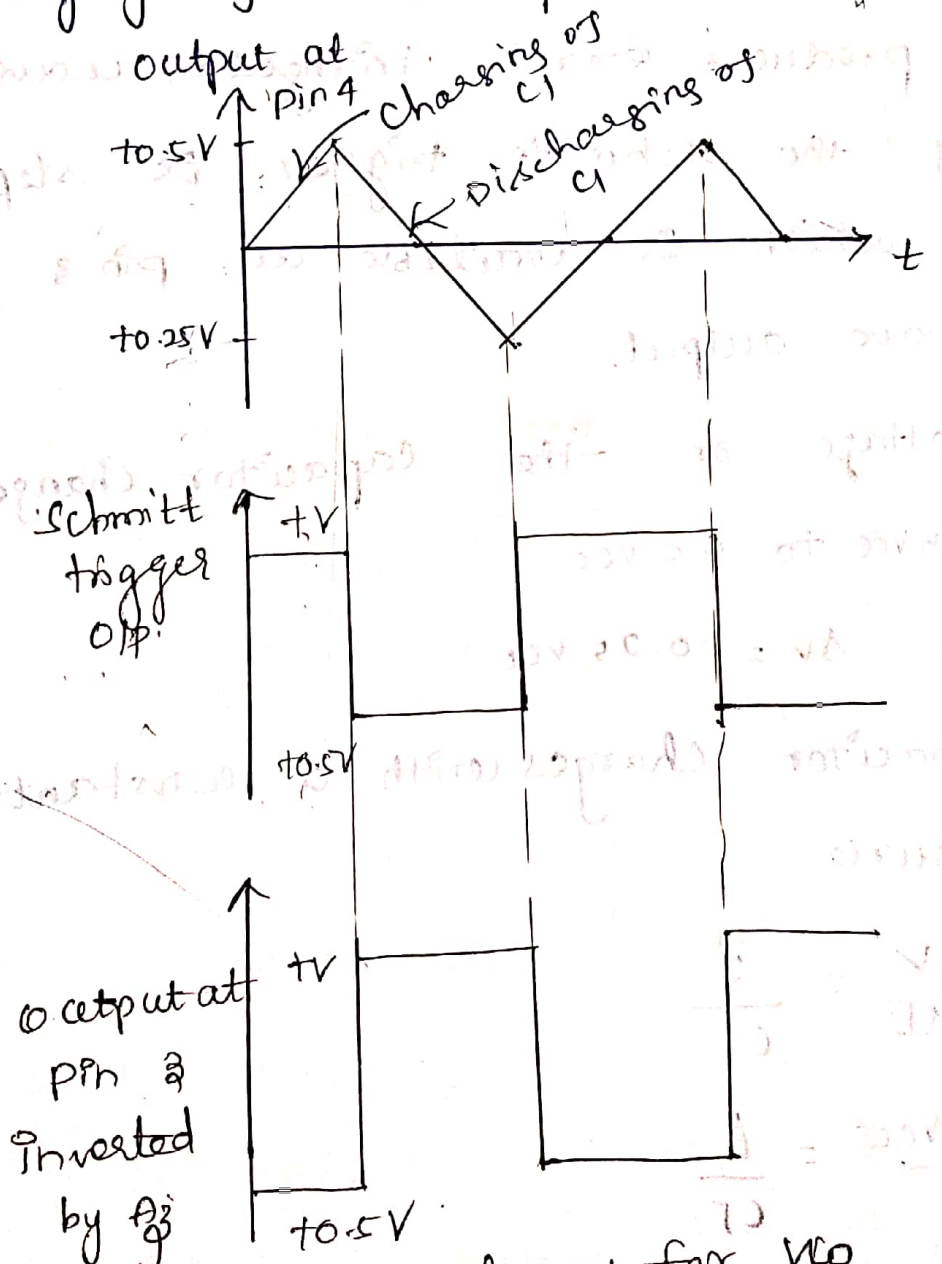


Block diagram.

The op-amp A_1 is used as a buffer. The op-amp A_2 is used as a schmitt triggers and A_3 is used as an inverter. The

voltage V_C is applied to the modulation input pin 5 which is a control voltage.

The output voltage of schmitt trigger is designed to swing between +V and 0.5V. For $R_A = R_B$ the voltage at non inverting terminal swings between 0.5(+V) to 0.25 (+V). Thus the triangular wave is generated due to alternate charging and discharging of the capacitor C_1 in linear manner.



waveforms for VCO

20

When C_1 voltage increases beyond 0.5(+V), the schmitt trigger output goes low and the capacitor starts discharging.

When the voltage becomes less than 0.25(+V) the output of the schmitt trigger goes high. Due to similar current sources used for charging and discharging the time taken by C_1 to charge and discharge is same.

This produces exact triangular wave. The output of the schmitt trigger is step response which is available at pin 3 as a square wave output.

The voltage of the capacitor changes from 0.25 Vcc to 0.5 Vcc

Thus $\Delta V = 0.25 V_{cc}$.

The capacitor charges with a constant current source.

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\therefore \Delta t = \frac{0.25 V_{CC} C_T}{i}$$

The time period T of the triangular waveform = $2\Delta t$.

The frequency of oscillator f_o is

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{1}{2\left(\frac{0.25 V_{CC} C_T}{i}\right)}$$

$$f_o = \frac{i}{0.5 V_{CC} C_T}. \qquad i = \frac{V_{CC} - V_c}{R_T}$$

But $$i = \frac{V_{CC} - V_c}{R_T}$$

V_c is the voltage at pin 5.

$$\therefore f_o = \frac{(V_{CC} - V_c)}{0.5 V_{CC} R_T C_T}$$

$$f_o = \frac{2(V_{CC} - V_c)}{R_T C_T V_{CC}}$$

The output frequency of the VCO can be changed either by

i) R_T ii) C_T iii) the voltage V_c at the modulating input terminal pin 5.

7.2. Voltage to Frequency Conversion factor :-

The voltage to frequency conversion factor is an important factor of IC 566. It is denoted as K_V.

$$K_V = \frac{\Delta f_o}{\Delta V_c}.$$

ΔV_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO.

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If we assume that the original frequency is f_o and the new frequency is f_1 then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - V_C + \Delta V_C)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - V_C)}{C_T R_T V_{CC}}$$

$$\Delta f_o = \frac{2 \Delta V_{CC}}{C_T R_T V_{CC}}.$$

(or) $$\Delta V_C = \frac{\Delta f_o C_T R_T V_{CC}}{2}. \quad \text{---------- (1)}$$

With no modulating input signal, if the voltage at Pin 5 is biased at $(4/8)V_{CC}$. then the VCO o/p frequency is

$$f_o = \frac{2(V_{CC} - 4/8 V_{CC})}{C_T R_T V_{CC}}$$

$$= \frac{2 (1/8 V_{CC})}{C_T R_T V_{CC}}$$

$$= \frac{V_{CC}}{4 R_T C_T V_{CC}}$$

$$f_o = \frac{0.25}{R_T C_T} \quad \text{---------- (2)}$$

$$\Rightarrow R_T C_T = \frac{0.25}{f_o} \quad \text{---------- (3)}$$

Substitute the value of $R_T C_T$ in eqn ①.

$$\Delta V_C = \frac{\Delta f_o \, V_{CC} \, 0.25 f_o}{f_o \times 2}$$

$$\Delta V_C = \frac{\Delta f_o \, V_{CC} \, 0.125}{f_o}$$

$$K_V = \frac{\Delta f_o}{\Delta V_C} = \frac{f_o}{0.125 V_{CC}}$$

$$\boxed{K_V = \frac{8 f_o}{V_{CC}}}$$

7.3 Features of 566 VCO :-

1) wide supply voltage range 10V to 24V
2) very linear modulation characteristics
3) High temperature stability.
4) Excellent power supply rejection.
5) 10 to 1 frequency range with fixed C_1.
6) The frequency can be controlled by means of current, voltage, resistor or capacitor.

9.7.4 Applications of VCO

1) FM modulation
2) Signal generation (Triangular or Square wave)
3) Function generation.
4) Frequency shift keying.
5) In frequency multiplier.
6) Converting low frequency signals such as EEG and EKG into audio frequency range signals.
7) Tone generation.

4.4.B High speed sample and Hold circuit:

For accurate analog to digital conversion the analog input voltage should be held constant during the conversion cycle.

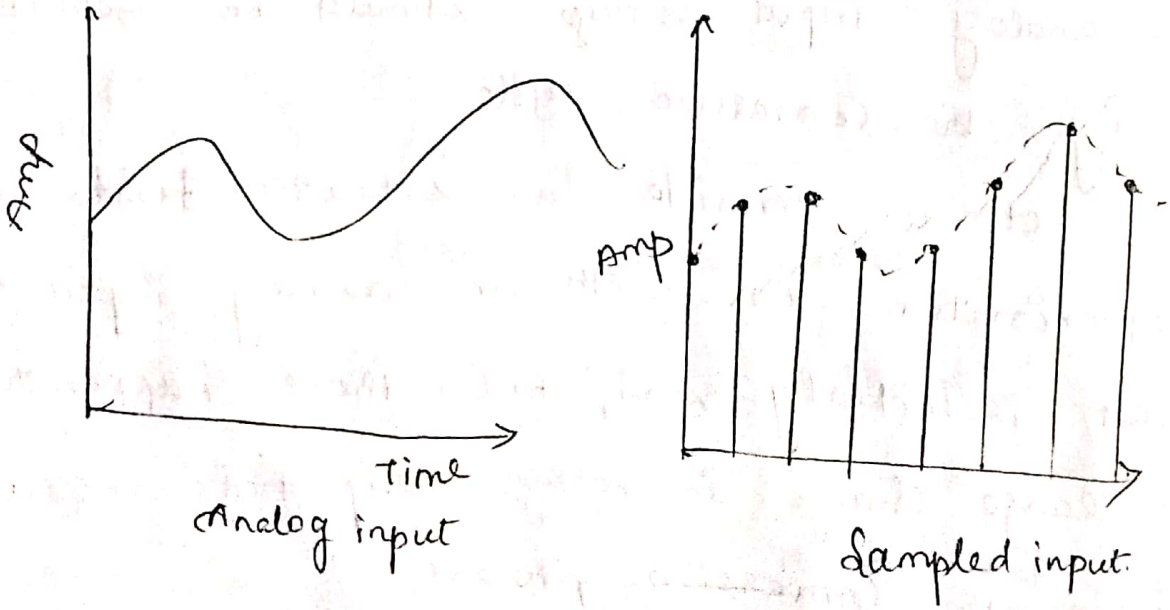
Let us consider a situation of a successive approximation ADC with an analog input voltage that is initially zero, but there happen to be a large change in voltage amplitude occuring during the conversion process.

Analog input voltage at start of conversion process is zero volts and at the end of

Conversion process it is near to 1.5 volts and the conversion process result is 010 (ie) 2.5 V. This result does not corresponds to the analog voltage at the start of conversion or at the end of conversion.

To minimise the occurrence of these errors it is necessary to hold the value of the analog input voltage over constant during the conversion process. The sample hold circuit does this task.

The sample and hold circuit samples the value of the input signal in response to a sampling command and hold it at the output until arrival of the next command.



Analog input

Sampled input

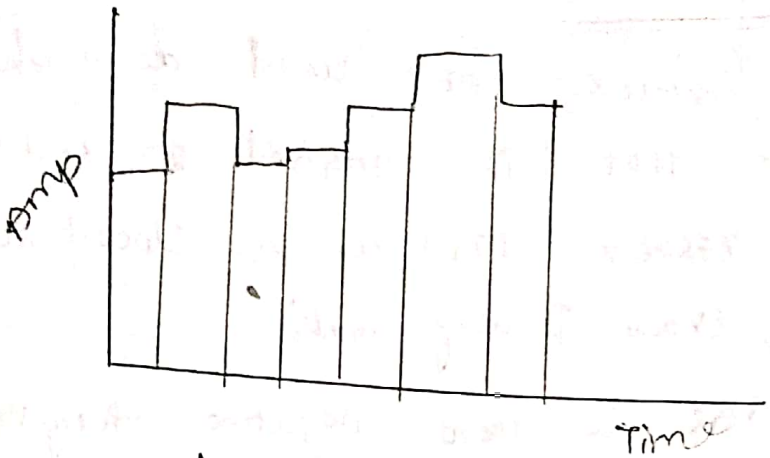


Fig: 4.4 I/p and o/p response of sample and hold circuit.

The sample and hold circuit uses basic components such as analog switch and capacitor

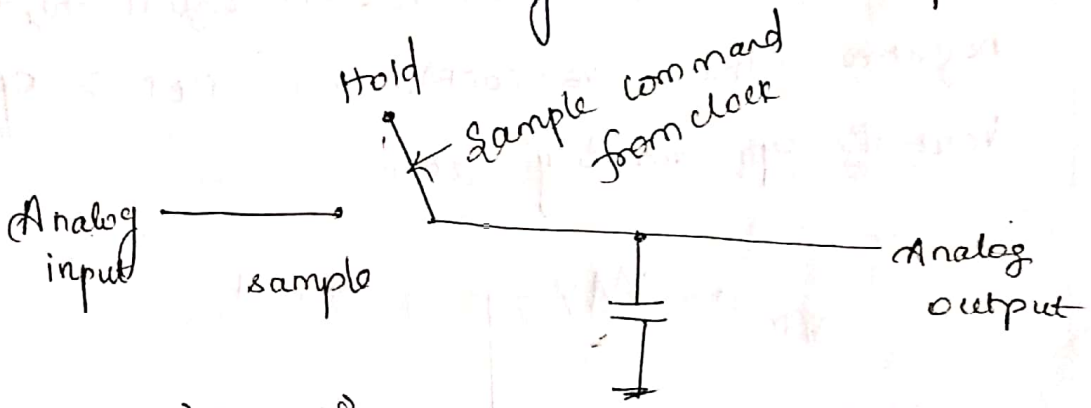


Fig: 4.4.2 principle diagram for sample and hold circuit

The circuit tracks the analog signal until the sample command causes the digital switch to isolate the capacitor from the signal, and the capacitor holds the analog voltage during A/D conversion.

4.4.1 Analog switches:

JFET can be used as an analog switch. For this the gate source voltage V_{GS} is restricted to two values: 0V or a large negative voltage.

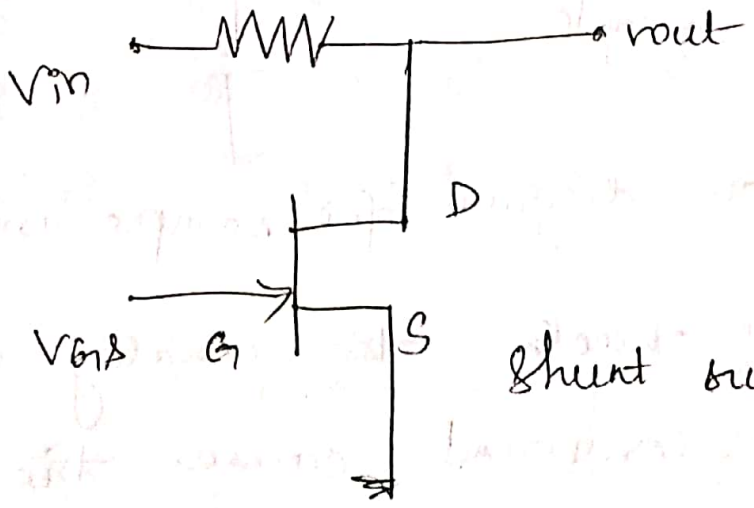
4.4.1.1 Shunt switch:-

Figure shows JFET used as a shunt switch. The JFET is turned on and off by V_{GS}. When $V_{GS} = 0$ V, JFET as a closed switch $R_{DS} \ll R_D$. (V_{out} is very small)

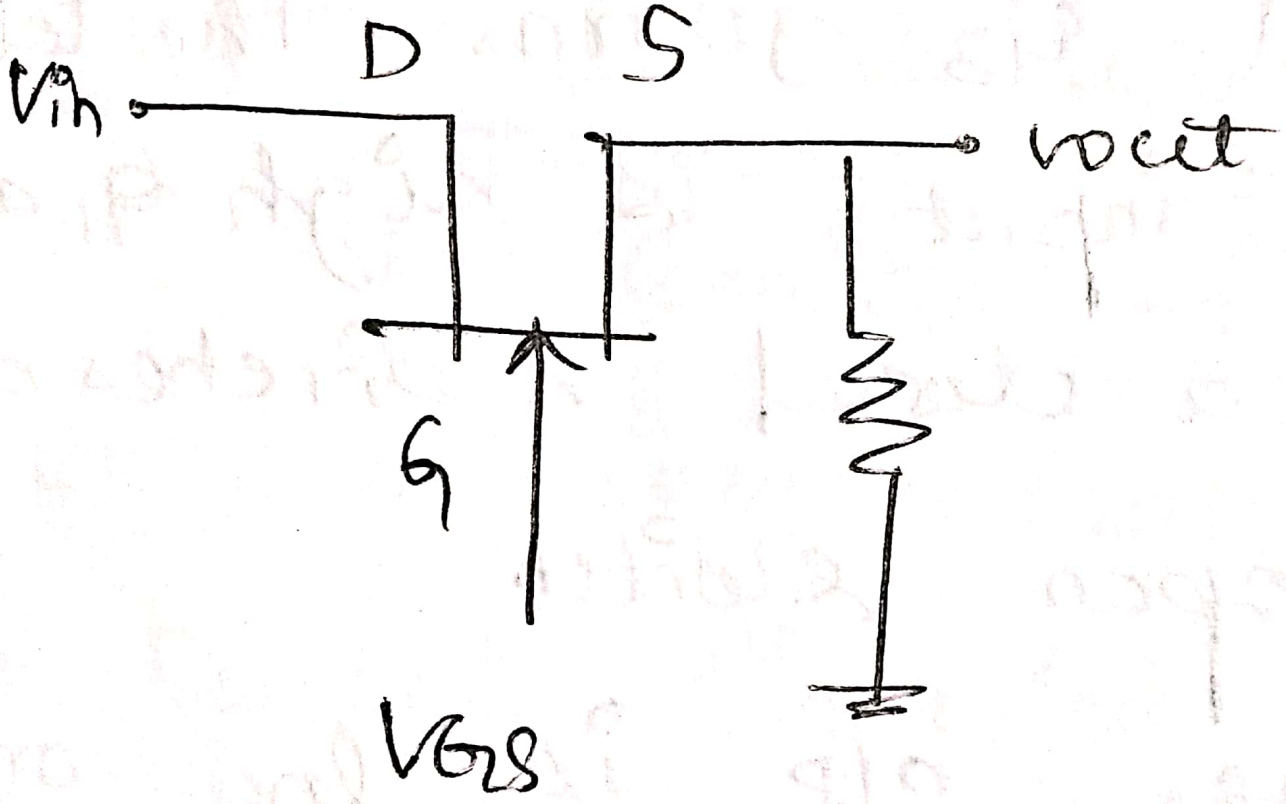
When V_{GS} is more negative than $V_{GS(OFF)}$ the JFET acts as an open switch. ($V_{out} = V_{in}$)

4.4.1.2 Series switch:-

When $V_{GS} = 0$, the switch is closed and V_{out} equals V_{in}. When V_{GS} is equal to, or more negative than $V_{GS(OFF)}$, the JFET is open and V_{out} is approximately zero.



Shunt switch



Series switch

4.4.2 Sample and Hold Circuits :-

Here JFET is used as switch. During the sampling time the JFET switch is turned on, and the holding capacitor charges up to the level of analog input voltage.

At the end of this short sampling period, the JFET switch is turned off.

this isolates the holding capacitor C_H from the input signal.

As a result the voltage across capacitor C_H and hence the o/p voltage will remain essentially constant at the value of the input voltage at the end of the sampling time.

However, there will be a small drop off or drop of the capacitor voltage during the hold period due to the various leakage currents. To avoid this, i/p and o/p buffers (voltage follower) circuits are used.

Figure shows the open loop architecture of the sample and hold circuit.

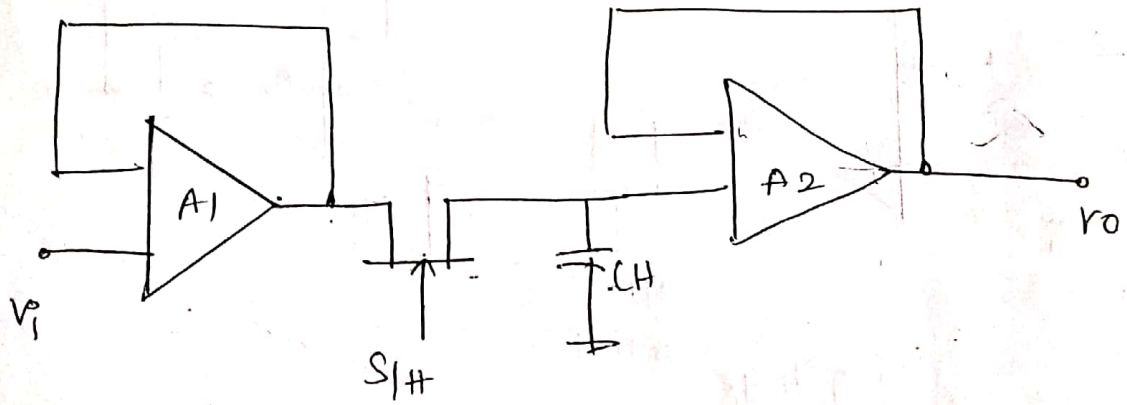


Fig: 4.4.7

The open loop type sample and hold circuits are faster than closed loop type which have delayed o/p feedback to the input buffer.

Acquisition time :

It is the time required for the holding capacitor C_H to charge up to a level close to the i/p voltage during sampling.

It should be as low as possible.

There are three principle factors that will control the acquisition time

i) RC time constance

R → resistance of JFET (r_{ds})

C → holding capacitance C_H.

2) Maximum o/p current given by the op-amp.

3) slew rate of the op-amp

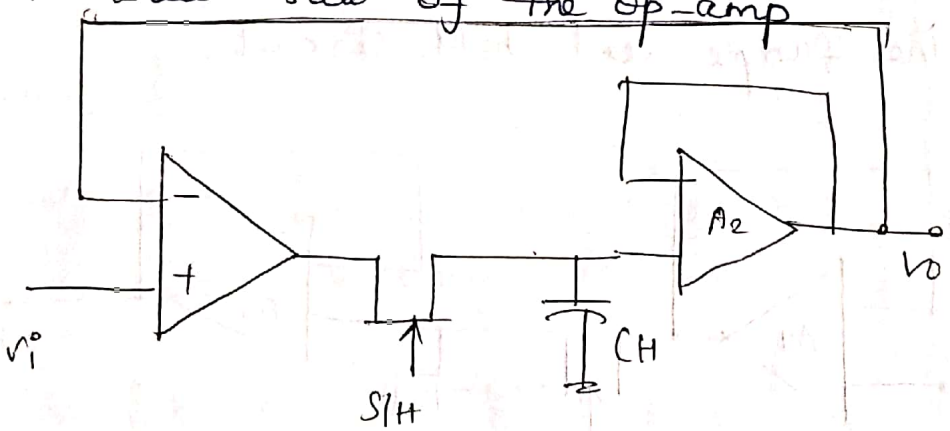


fig 4.48

The above circuit has some advantages in terms of acquisition time.

Since the r_{ds} (on) of the JFET switch is inside the feedback loop of A1. Therefore the acquisition time for this circuit is limited by maximum o/p current and slew rate of

the Op-amp, rather than the RC time constant.

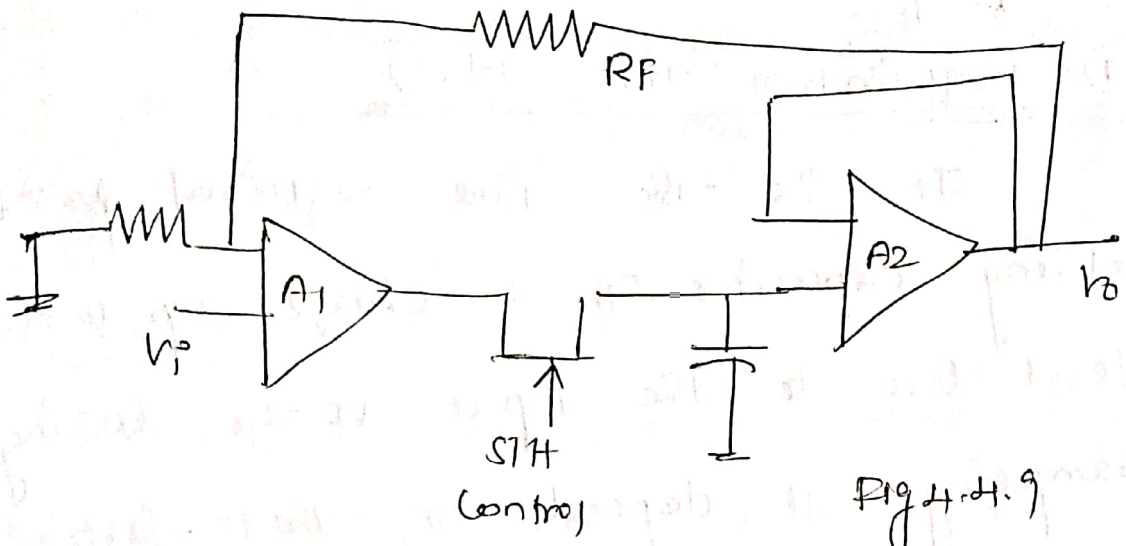


Fig 4.4.9

The above S/H circuit offers the additional feature of providing voltage gain.

$$A = 1 + \frac{R_F}{R_1}$$

∴ The sampled O/P voltage is equal to the sampled input voltage multiplied by voltage gain factor of $1+(R_F/R_1)$.

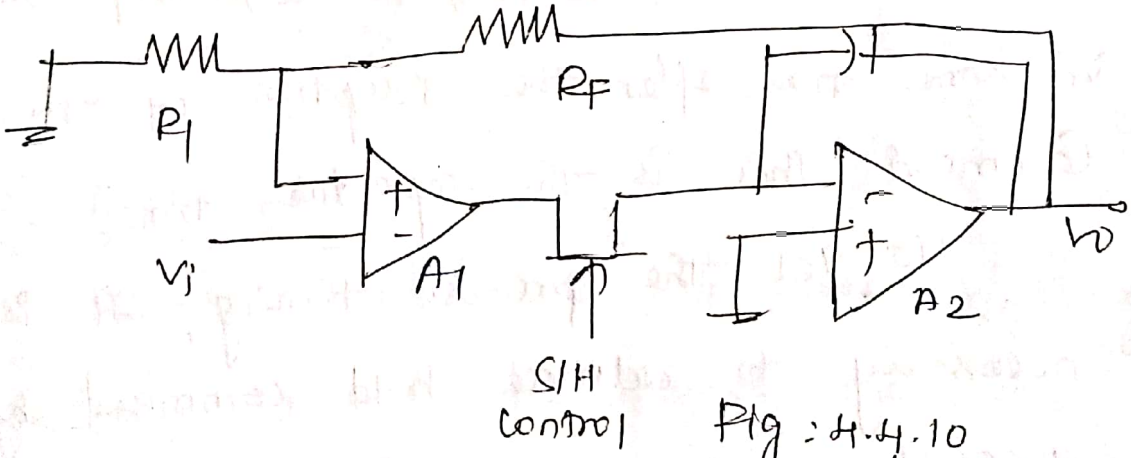


Fig : 4.4.10

This S/H circuit offers two advantages.

1) The faster charging capacitor rate provides shorter acquisition time.

4.4.3 performance parameters of S/H circuit.

1) Acquisition time (tac)

It is the time required for the holding capacitor CH to charge up to a level close to the input voltage during sampling. It depends on three factors

1) RC time constant.
2) Maximum o/p current of op-amp
3) Slew rate of op-amp.

2. Aperture time (tap)

Because of propagation delays through the driver and switch, it will keep tracking VI some time after the inception of the hold command. this is the aperture time.

To get the precise timing, It is necessary to advance hold command by this amount.

3. Aperture uncertainity (Δtap).

It is the variation in aperture time from sample to sample.

4. Hold mode settling time (ts)

After the application of hold command,

it takes a certain amount of time for V_o to settle with in a specified error band such as 1%. 0.1% or 0.01%. This is the hold mode settling time.

b) Hold step :-

Because of the parasitic switch capacitance at the time of switching between sample to hold mode, there is an unwanted transfer of charge between the switch driver to C_H.

This charges the capacitor voltage and hence the output voltage.

This charges in output voltage are referred to as hold step.

$$\Delta V_o = \frac{\Delta Q}{C_H}.$$

6) Feed through :

In the hold mode, because of stray capacitance across the switch, there is a small amount of ac coupling between V_o and V_i.

This ac coupling causes the output voltage to vary with variation in the input voltage.

$$\Delta V_o = \frac{C_{ds}}{C_H} \Delta V_i$$

C_{ds} → Stray capacitance between drain and source of JFET.

Feedthrough is usually expressed in terms of feedthrough rejection ratio (FRR) and it is given as

$$FRR = 20 \log_{10} \frac{\Delta V_i}{\Delta V_o}$$

7) Voltage droop :-

The leakage current causes voltage of the capacitor to drop down. This is referred to a droop.

4.4 Advantages of sample and Hold Circuits

1. The primary use of the sample and hold circuit is to hold the sampled analog input voltage constant during conversion time of A/D Converter.

2) It reduces the crosstalk in the multiplexer.

3) In case of multichannel ADCs, synchronization can be achieved by sampling signals from all channels at the same time.

4.4.5 Applications of sample and Hold circuits :-

1) Digital interfacing
2) Analog to digital Converter circuits.
3) pulse modulation systems.
4) In analog demultiplexers.

4.2.2 Types of D/A converter :

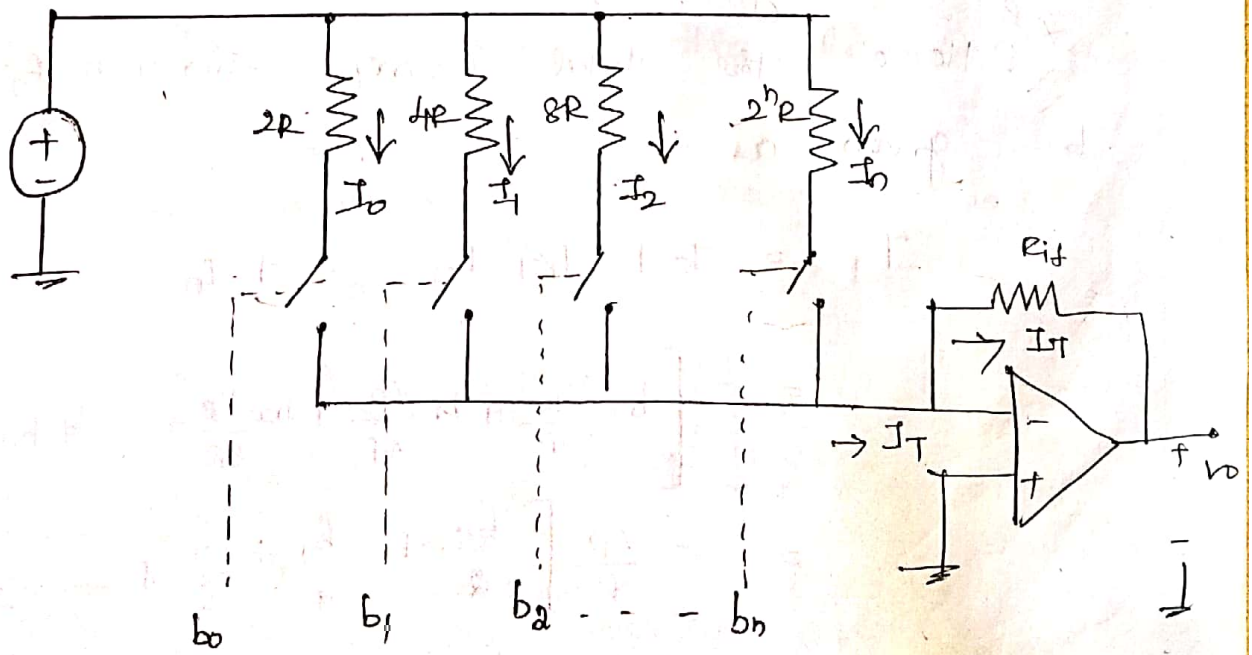
There are mainly two techniques used for Digital to analog conversion

1) Binary weighted resistor D/A Converter.
2) R/2R ladder D/A converter.

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input.

Therefore such digital to analog converters are called current driven DAC's.

4.2.1 Binary weighted resistor D/A converter :



Here n = 4.

Fig : 4.2.2.

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors $2R, 4R, 8R, \ldots 2^nR \ldots$

The switch positions are controlled by the digital inputs. When the digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R. otherwise it leaves resistor open.

For open (ON) switch $I = \frac{V_R}{R}$ and

For OFF switch $I = 0$

Operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_f.

Hence the total current through R_f can be given as

$$I_T = I_0 + I_1 + I_2 \ldots + I_n$$

$$= -\left[b_0 \frac{V_R}{2R} + b_1 \frac{V_R}{4R} + b_2 \frac{V_R}{8R} + \ldots + b_n \frac{V_R}{2^nR} \right] R_f$$

$$= -\frac{V_R}{R}\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \ldots \frac{b_n}{2^n} \right] R_f$$

$$= -\frac{V_R}{R} R_f \left[b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \ldots b_n 2^{-n} \right]$$

when $R_f = R_1$, V_o is given by

$$V_o = -V_R \left(b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \dots b_n 2^{-n} \right)$$

The above equation indicates that the analog O/P voltage is proportional to the input digital word.

Drawbacks:

1) Wide range of resistor values are required. For 8bit DAC, the resistors required are 2^1R, 2^1R, 2^2R, 2^3R and 2^8R. Therefore the largest resistor is 128 times the smallest one.

2) It is impracticable to fabricate large values of resistor in IC, the voltage drop across such a large resistor due to the bias current also effects the accuracy. For smaller values of resistors, the loading effect may occur.

The requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8 bits.

4.2.2.2 Inverted R-2R ladder/ current mode R-2R ladder D/A Converter:-

R/2R ladder D/A Converter uses only two resistor values. This avoids the drawback of

binary weighted D/A converter. Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents. However it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC.

Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes.

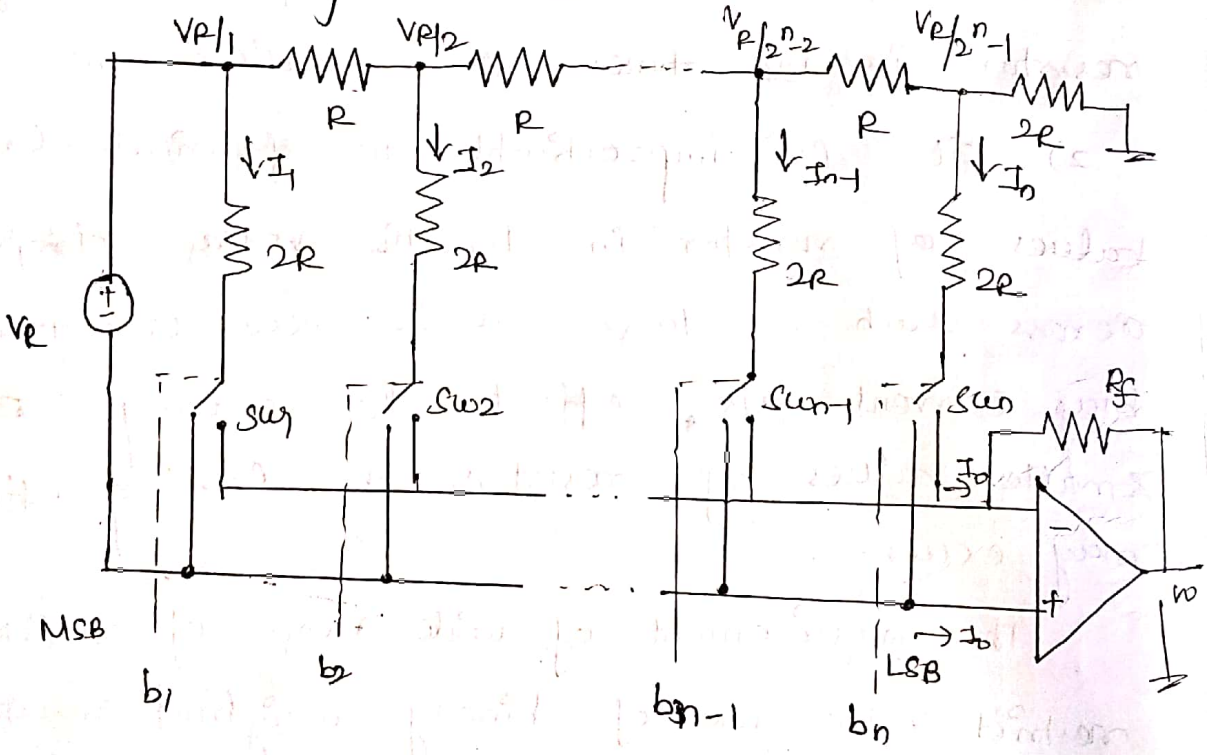


Fig 4.2.3 Current mode R-2R ladder type.

Here each bit of the binary word Connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground,

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

$$V_0 = -I_f R_f$$

$$= -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

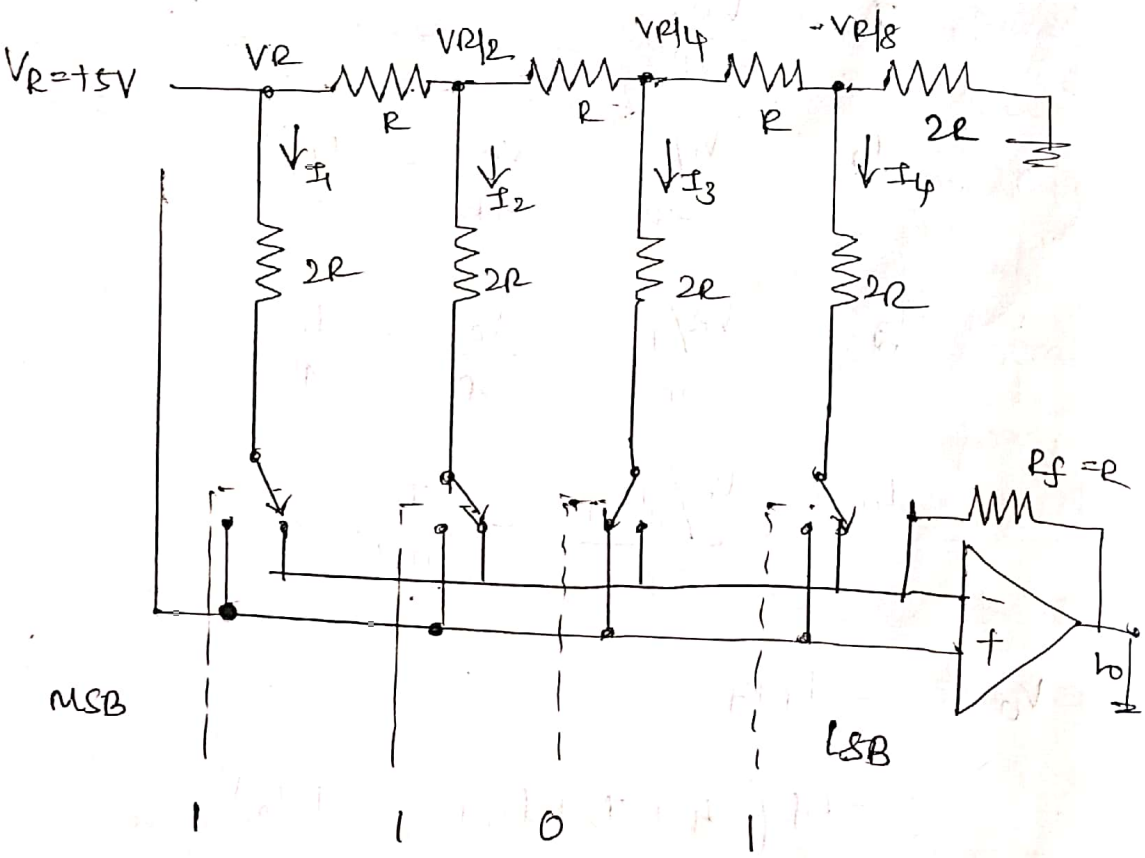
$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots b_n \frac{V_R}{2^n R} \right)$$

$$= -\frac{V_R R_f}{R} \left(b_1 2^{-1} + b_2 2^{-1} + b_3 2^{-3} + \cdots b_n 2^{-n} \right)$$

If $R_f = R$, v_0 is given as

$$V_0 = -V_R \left(b_1 2^{-1} + b_2 2^{-1} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)$$

Let us consides 4 bit binary DAC with binary input 1001 and $R_f = R$.



O/P voltage is given as

$$V_o = -V_R\left(1\times 2^{-1} + 1\times 2^{-2} + 0\times 2^{-3} + 1\times 2^{-4}\right)$$

$$= -V_R\left(\frac{1}{2} + \frac{1}{4} + 0 + \frac{1}{16}\right)$$

$$= -5\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16}\right)$$

$$V_R = -4.0625\ V$$

The inverting R/2R ladder DAC works on the principle of summing currents and it is also said to operate in the current steering mode.

4.2.2.3 R-2R ladder/ voltage mode R-2R ladder D/A Converter :-

In this type, Reference voltage is applied to one of the switch positions and other switch position is connected to ground.

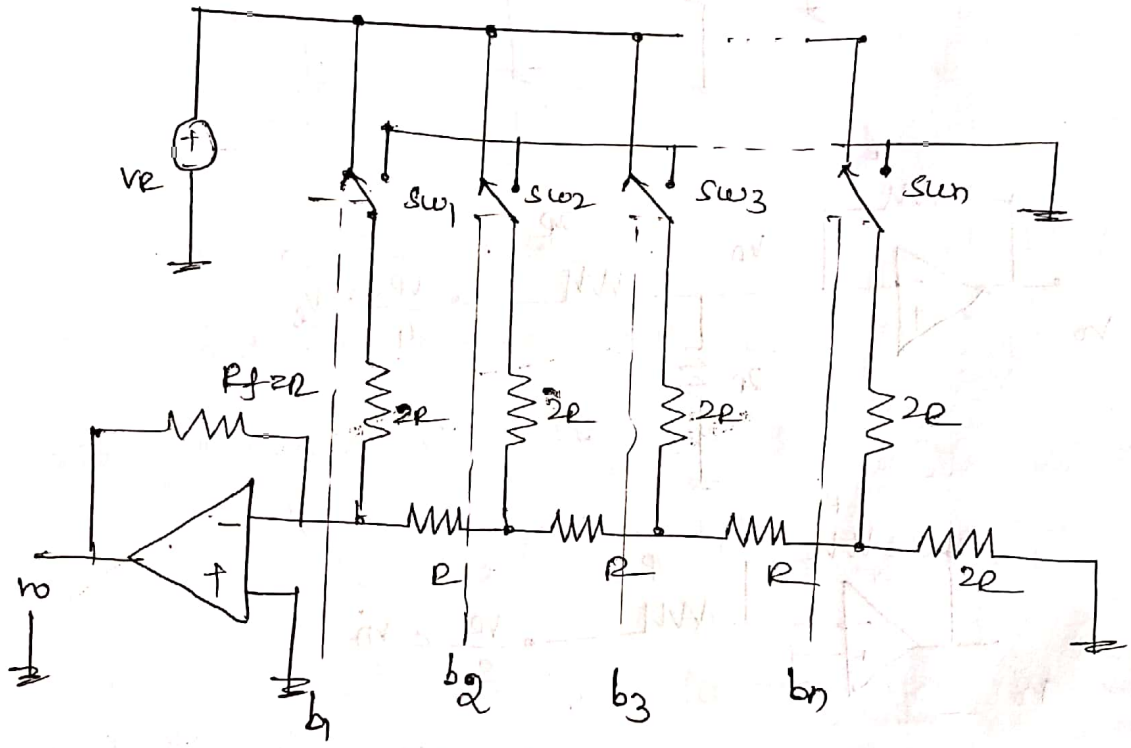
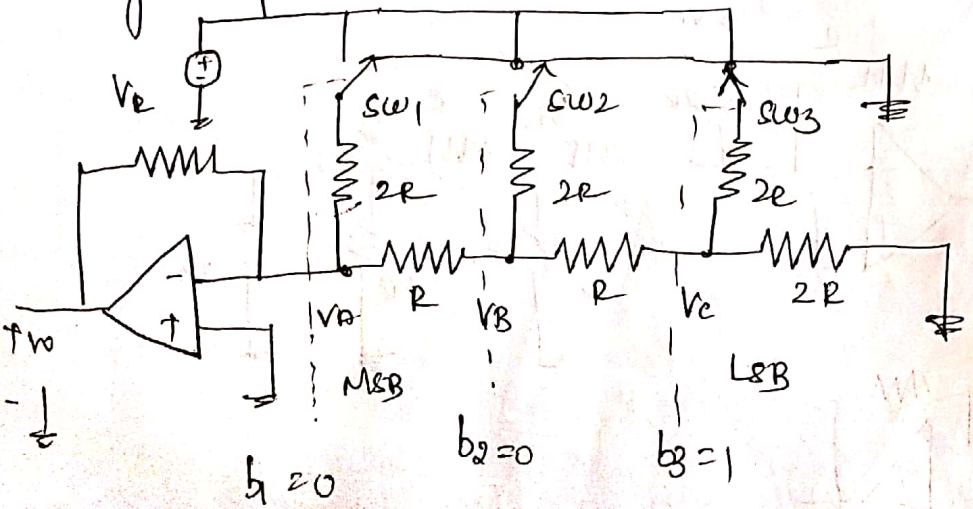
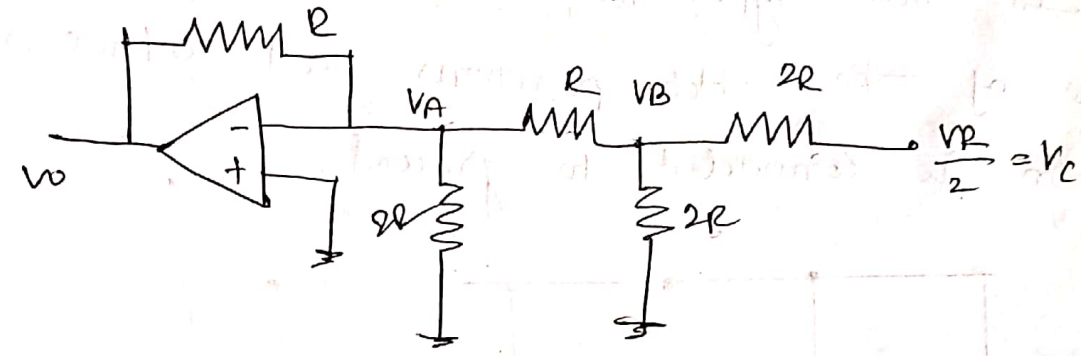


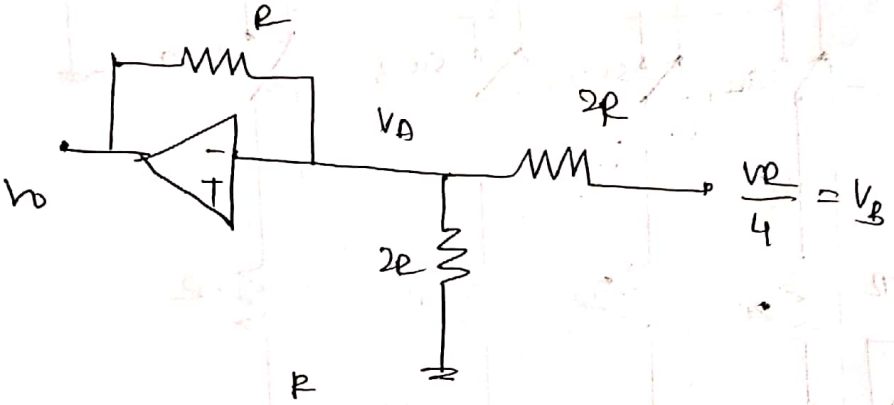
Fig 4.2.4 R/2R ladder D/A Converter.

Let us consider 3-bit R/2R ladder DAC with binary input 001



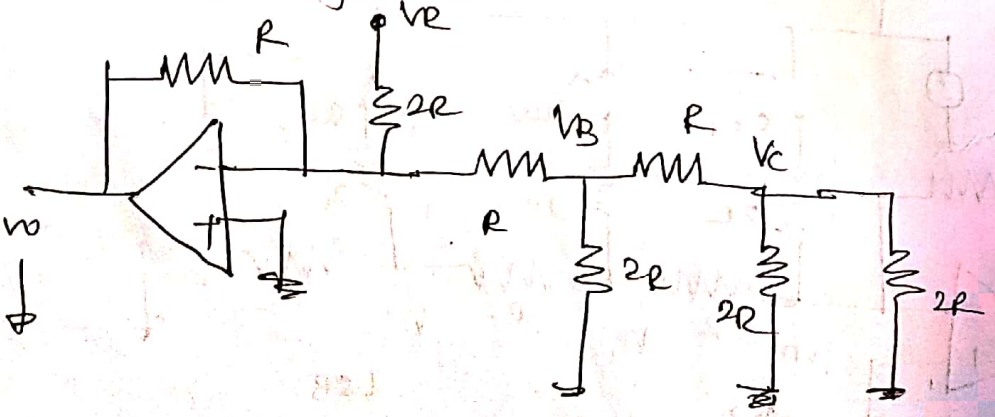
Reducing above network to the left by Thevenin's theorem we get

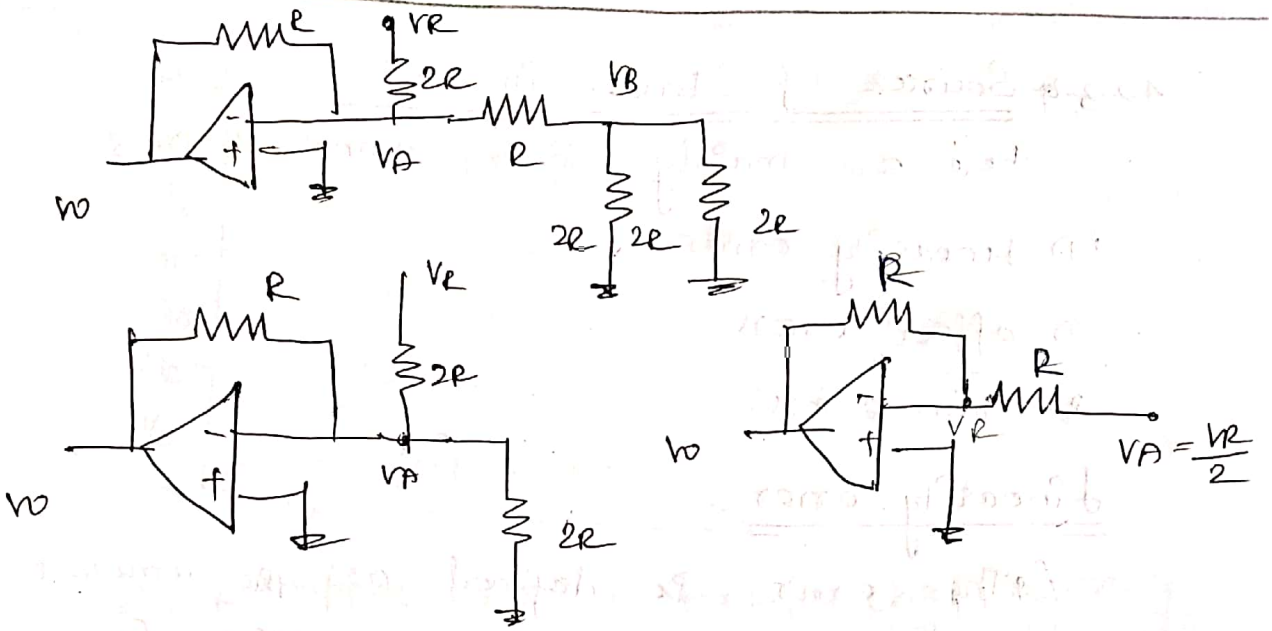




Therefore the output voltage is $\frac{V_R}{8}$ which is equivalent to binary input 001.

For binary input 100 the network can be reduced as follows:





∴ The output voltage is $\frac{V_R}{2}$ which is equivalent to binary input 100.

In general the voltage is given by

$$V_0 = -V_R \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n} \right)$$

The resolution of R/2R ladder type DAC with voltage output is

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R} \right) \times R_f .$$

Advantages :-

1. Easier to build accurately as only two precision metal film resistors are required.
2. No of bits can be expanded by adding more sections of same R/2R values.

4.2.1 performance parameters of DAC:-

The various performance parameters of DAC are

1) Resolution
2) Accuracy
3) Monotonicity
4) Conversion time
5) Settling time
6) Stability.

4.2.1.1 Resolution

Resolution of a Converter is the smallest change in voltage which may be produced at the output of the Converter.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1}$$

It is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs.

V_{FS} = Full scale output voltage.

For an 8 bit DAC resolution can be given as Resolution $= 2^n = 2^8$

$= 256$

If the full scale o/p voltage is 10.2 V then the resolution for an 8bit DAC can be given as

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{10.2}{2^8 - 1}$$

$$= \frac{10.2}{255}$$

$$= 40\,mV/LSB$$

4.2.1.2 Accuracy:

It is a comparison of actual output voltage with expected output. It is expressed in percentage.

If the full scale output voltage is 10.2 V then for an 8 bit DAC accuracy can be given as

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n - 1)2}$$

$$= \frac{10.2}{255 \times 2} = 20\,mV.$$

4.2.1.3 Monotonicity:

A monotonic DAC is the one whose analog output increases for an increase in digital output.

A converter is said to have good monotonicity if it does not miss any step

backward when stepped through its entire range by a counter.

4.2.1.4 Conversion time :

It is a time required for conversion of analog signal into its digital equivalent. It is also called as setting time.

4.2.1.5 Settling time :

This is the time required for the output of the DAC to settle to with in ± 1/2 LSB of the final value for a given digital input (ie) zero to full scale.

4.2.1.6 Stability :

The performance of converters changes with temperature, age and power supply variations.

So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

These parameters represents the stability of the converter.

4.2.3.4 Sources of Errors in DAC

There are mainly three errors in DACs

1) linearity error
2) offset errors
3) Gain errors.

linearity error :-

The error is defined as the amount by which the actual output differs from the ideal straight line output.

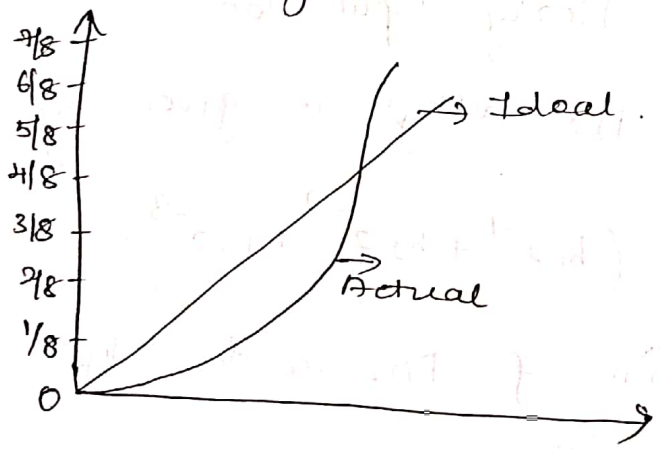


Fig: 4.25 linearity error in transfer characteristics of DAC.

Figure shows the linearity error in the transfer characteristics of DAC. It is mainly due to the errors in the current source resistor values.

Offset Error :-

The offset error is defined as the non zero level of the output voltage when all inputs are zero

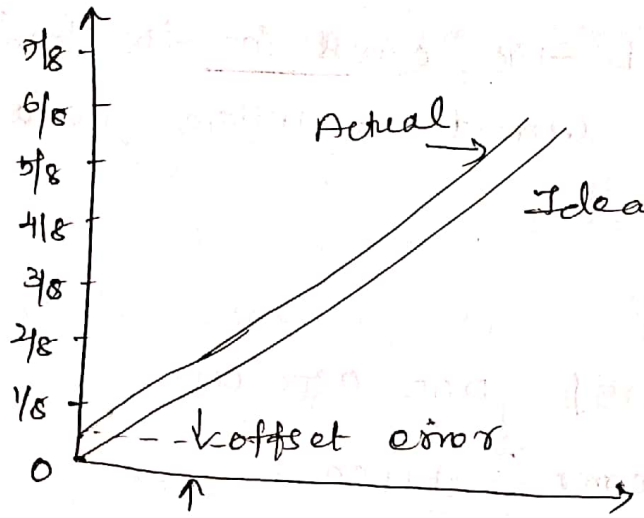


Fig: 4.2.6 Offset error in transfer characteristics of DAC.

It adds a constant value to all output values.

It is due to the presence of offset voltage in op-amp and leakage currents in the current switches.

Gain Error:-

The gain error is defined as the difference between the calculated gain of the current to voltage converter and the actual gain achieved.

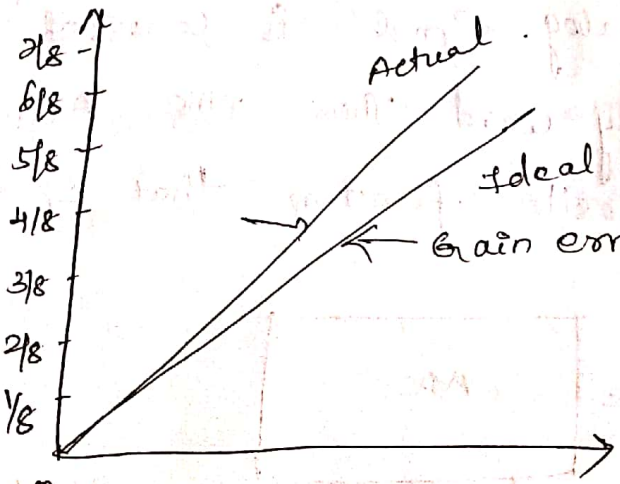


Fig 4.2.7 Gain error in transfer characteristics of DAC.

It is due to the errors in the feedback resistor or the current to voltage converter Op-amp.

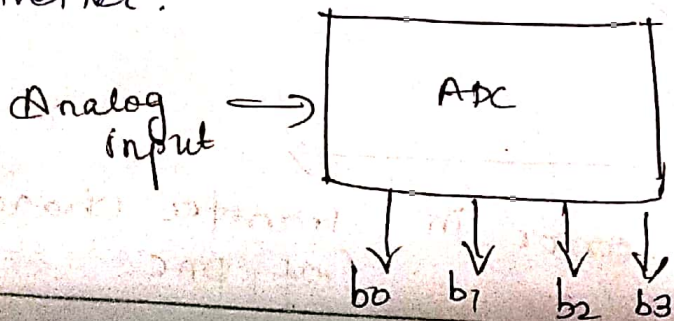
4.2.4 DAC 0800 :

The features of DAC 0800 are

1) Full scale error : ±1LSB
2) Nonlinearity over temperature : ±0.1%.
3) Wide power supply range : ±4.5V to ±18V
4) Low power consumption : 33mW at ±5V
5) Low cost.
6) Complementary current outputs.
7) Fast settling output current: 100ns.

4.3 A/D converters :

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function that of the D/A converter.



Symbol for 4 bit ADC.

4.3.1 Performance parameters of ADC:

4.3.1.1 Resolution:-

Resolution is defined as the ratio of a change in value of input voltage V_i needed to change the digital o/p by 1 LSB.

$$\text{Resolution} = \frac{V_{IFS}}{2^n - 1}$$

V_{IFS} → Full scale input voltage.

also $\text{Resolution} = 2^n$

4.3.1.2 Quantization error:-

$$Q_E = \frac{V_{IFS}}{(2^n - 1)\,2}$$

Its value is $\pm \frac{1}{2}$ LSB.

4.3.1.3 conversion time

It is defined as the total time required to convert an analog signal into its digital output.

It depends on the conversion technique used and the propagation delay of circuit components.

4.3.2 Basic Conversion techniques:

Analog to digital converters are classified into two general groups based on the conversion techniques.

One technique involves comparing a given analog signal with the internally generated reference voltage. this group includes

1) successive approximation
2) Flash type
3) delta modulated
4) Adaptive delta modulated converters.

The another technique involves changes an analog signal into time or frequency and comparing these new parameters against known values. This group includes

1) Integrator Converters
2) voltage to frequency converters.

In this chapter we are going to discuss the following types of ADCs using various conversion techniques.

1) Single slope ADC
2) successive approximation
3) Delta modulation.
4) Dual slope
5) Flash 6) Adaptive delta modulation.

The advantage of dual slope ADC are

1) It is highly accurate
2) Cost is low.

The disadvantage of fix ADC is

1) speed which is low.

4.3.2.3 : successive approximation ADC :-

successive approximation converter consists of a DAC, a comparator and a successive approximation register (SAR). The external clock input sets the internal timing parameter.

The control signal start of conversion (SOC) initiates an A/D conversion process and and of conversion signal is activated when the conversion is completed.

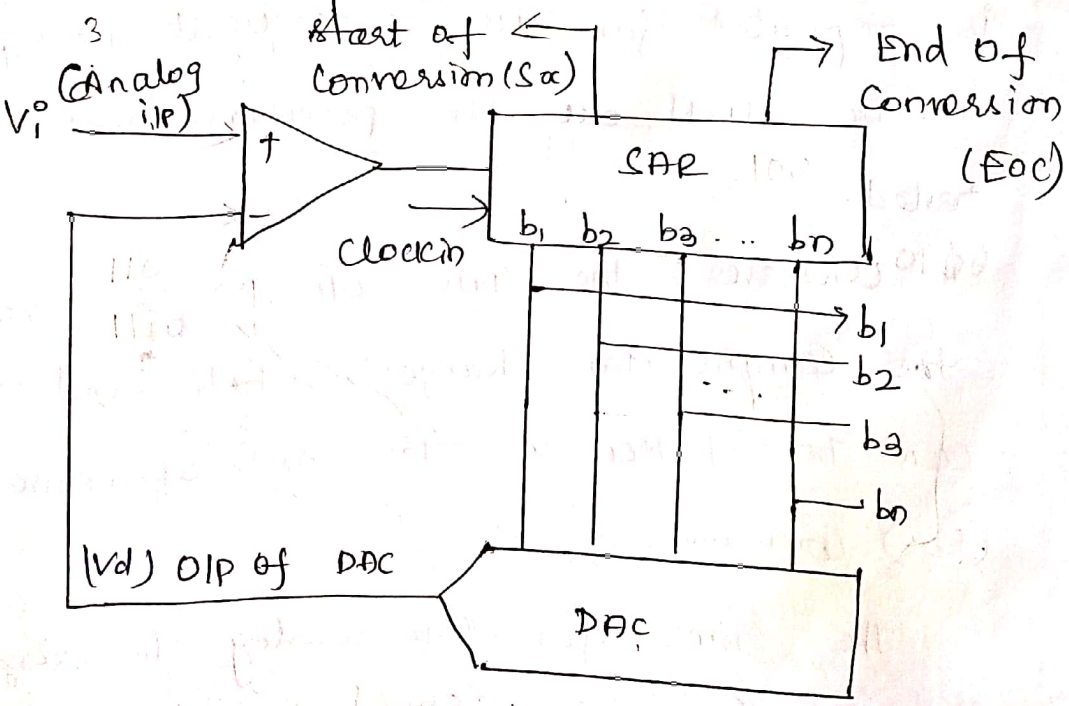


Fig:4.3.4 Block diagram of successive approximation A/D converter.

With the arrival of the start command, the SAR sets the MSB. $b_1 = 1$ with all other bits to zero, so that the trial code is 1000. The output Vd of the DAC is now compared with analog input Va. If Va is greater than the DAC output Vd then 1000 is less than the correct digital representation. The MSB is left at 1 and the next lower significant bit is made 1 and further tested.

If Va is less than the DAC output then, 1000 is greater than the correct digital representation. So reset MSB to 0 and go on to the next LSB. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.

Whenever the DAC O/P crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command.

The time for one analog to digital conversion must depend on both the clock's period T and number of bits n. It is given as

Example :

Correct digital input	output Vd at different stages	Comparator o/p
1101 (13)	1000 (8)	1 (Initial o/p)
	1100 (12)	1
	1110 (14)	0
	1101 (13)	
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

$T_C = T(n+1)$

$T_C \rightarrow$ Conversion time

$T \rightarrow$ clock period

$n \rightarrow$ no of bits.

Successive Approximation Algorithm.

take $V_{in} = 3V$

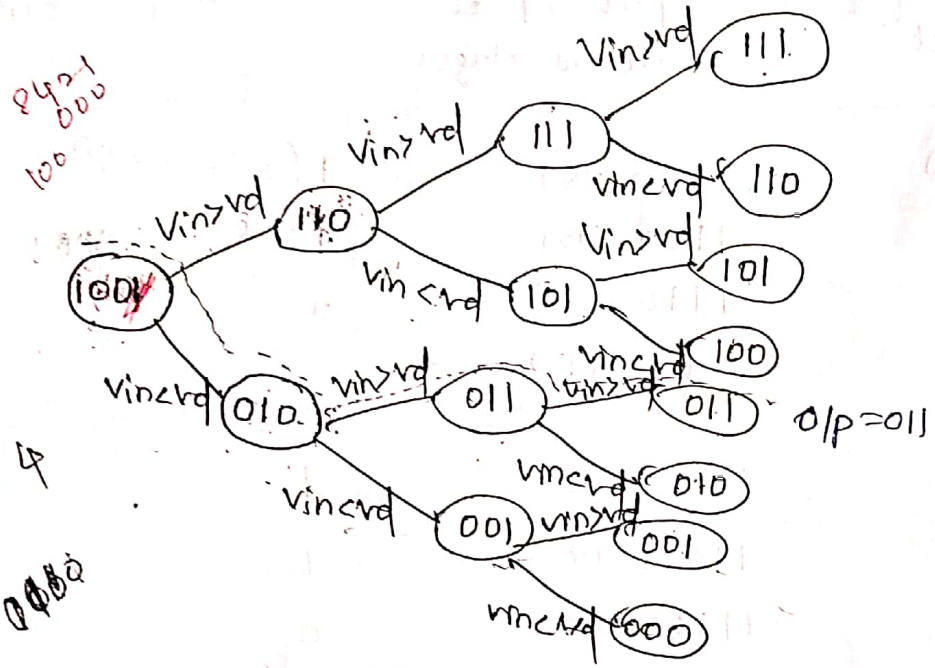


Fig : 4.3.5

3 X 8

$V_{in} > V_d$ = set MSB as 1

$V_{in} < V_d$ = Reset the Already set bit and set the next bit.

It needs 3 clock pulses to Convert 3 bit digital data.

If we have 4 bit digital data then it needs 4 clock pulses.

So a n bit converter needs n clock pulses to convert it into digital form.

Vin = 13V (1101)

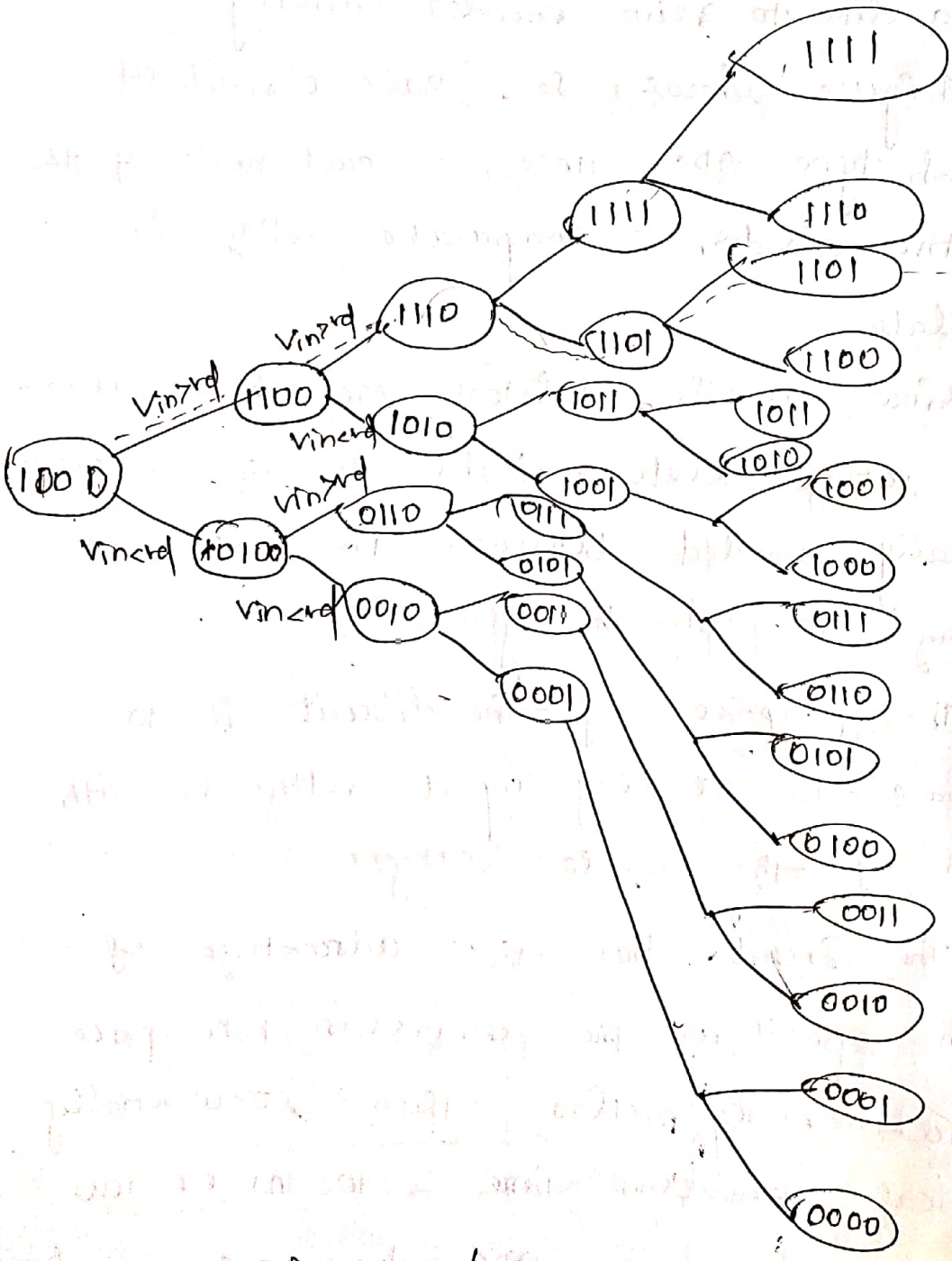


Fig: 4.3.6

4.3.2.4 Flash Type ADC :- (Parallel Type ADC)

This the simplest possible A/D converter. At the same time, the fastest and most expensive technique. The circuit consists of a resistive divider network, $2^n - 1$ comparators and a 8 line to 3 line encoder (priority encoder).

Figure shows the Basic circuit of Flash type ADC. Here, at each node of the resistive divider, a comparator voltage is available.

Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground.

The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages.

The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit.

A 2bit ADC requires $2^2 - 1 = 3$ comparators, 3 bit ADC needs 7, whereas 4 bit requires 15 comparators.

In general, the no of comparators required are $2^n - 1$ where n is the desired no of bits.

Also the larger value of n, the more Complex is the priority encoder.

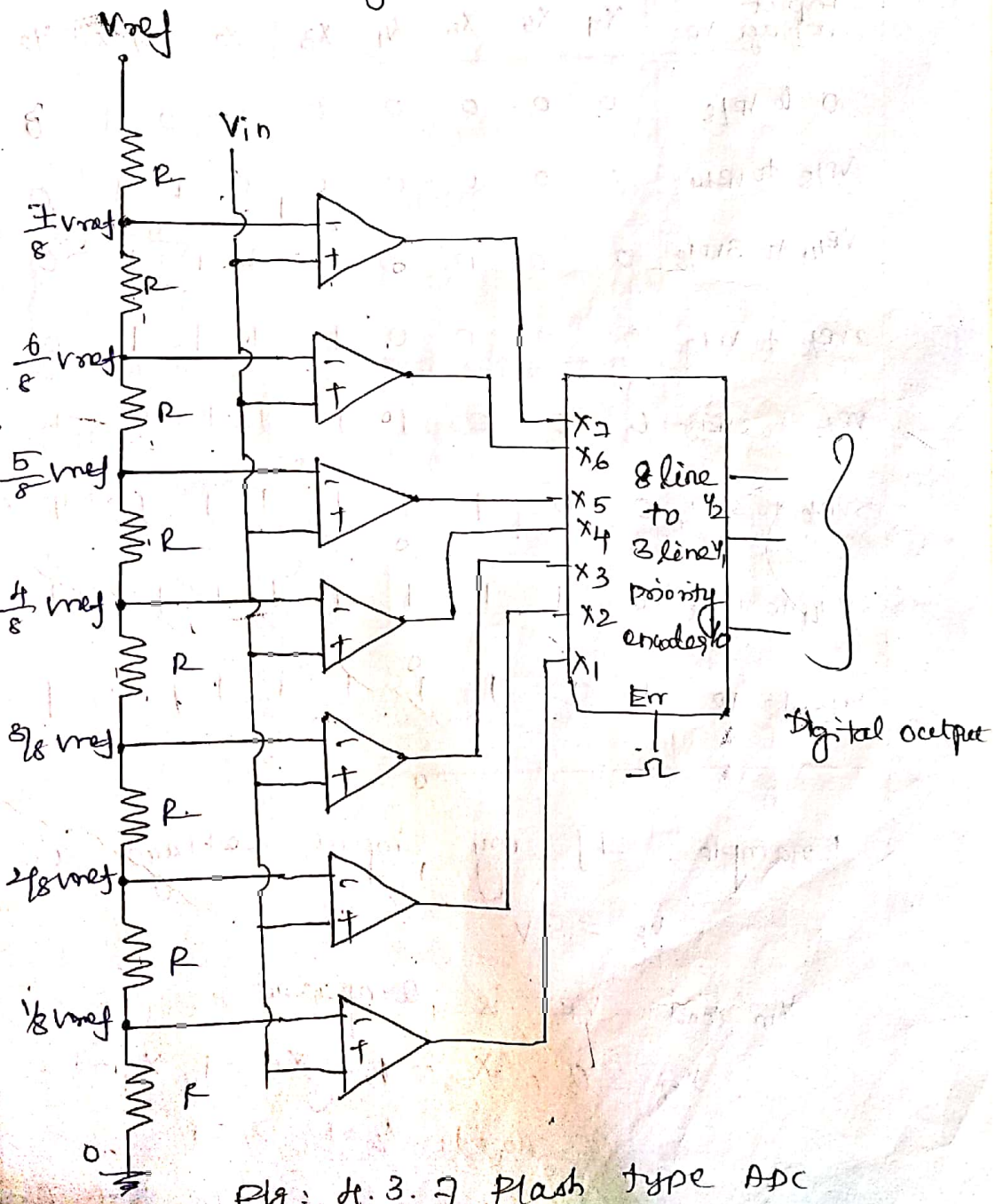


Fig: 4.3.7 Flash type ADC

Voltage input	logic output x
$V_a > V_d$	$x = 1$
$V_a < V_d$	$x = 0$
$V_a = V_d$	previous value

Comparator and its truth table.

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to $3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to $5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8$ to $3V_R/4$	0	0	1	1	1	1	1	1	1	0	1
$3V_R/4$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Example: If my input voltage as 6V.

$V_R = 8V$.

V_{in} and V_R is compared

$\therefore$ $X_7 = 0$, $X_6 = 0$, $X_5 = 1$, $X_4 = 1$

$X_3 = 1$, $X_2 = 1$ $X_1 = 1$

For 0 1 1 1 1 1 input the O/P of priority

Encodes will be 110

4.8.2.5 Comparison between Flash, Dual slope and successive approximation techniques:

parameter	Flash	successive Approximation	Dual slope
speed	Fastest	Fast	Slow
Accuracy	less	Medium	More
Resolution	upto 2^8	upto 2^{16}	2^{16} or even more
Cost	very less	Medium	less
Applications	High speed fiber optic communication, DSO,	Data acquisition systems	these are used when high accuracy and Resolution is required and speed is not the important criteria.

Problems :-

1) An 8 bit ADC is capable of accepting an input unipolar voltage 0 to 10V

a) what is the minimum value of input voltage to cause a digital o/p change of 1LSB?

b) what input voltage will cause all 1s at the ADC output?

c) what is the digital code if the applied i/p voltage is 5.2V?

Given : $V_{iFS} = 10V$.

a) $1LSB = \frac{V_{iFS}}{2^n} = \frac{V_{iFS}}{2^8} = \frac{10V}{28} = 39.1mV$

b) Minimum i/p voltage to cause all logic 1s at the output is = 10V - 39.1mV

= 0.961V.

c) $D = \frac{5.2V}{39.1mV} = 132.99 = 133$

Digital code = 10000101.

2) An 8 bit DAC has an o/p voltage range of 0 - 2.55V. Define its resolution in two ways.

i) Resolution $= 2^n = 2^8 = 256$.

ii) Resolution $= \frac{V_{FS}}{2^n - 1} = \frac{2.55}{2^8 - 1} =$ [illegible]

$= 10mV/1LSB$

Thus an input change of 1LSB causes the O/P to change by 10mV.

3) An 8bit DAC has resolution of 20mV/LSB Find V_{OFS} and V_O if the input is $(10000000)_2$

Given: Resolution = 20mV/LSB.

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

$$V_{OFS} = (\text{Resolution})\, 2^n - 1$$

$$= 20mV/LSB\,(2^8 - 1)$$

$$= 5.1V$$

$\boxed{V_{OFS} = 5.1V}$

$$V_O = \text{Resolution} \times D$$

$$= 20 \times 128 \times 10^{-3}$$

$$= 2.5V$$

$\boxed{V_O = 2.5V}$

4) Find out stepsize and analog O/P for 4 bit R-2R ladder DAC when i/p is 1000 and 1111. Assume $V_{ref} = +5V$.

For Given DAC $n=4$, $V_{OFS} = +5V$.

Stepsize = Resolution $= \frac{V_{FS}}{2^n - 1}$

$= \frac{5}{2^4 - 1}$

Stepsize = $\frac{1}{3}$ V/LSB

V_o = Resolution x D(1000)

$= \frac{1}{3} \times 8$

V_o = 2.6667V

V_o = Resolution x D(1111)

$= 1/3 \times 15$

V_o = 5V

Determine the Conversion time of 8bit & 16 bit successive approximation type ADC if its clock frequency is 50Hz. 100 KH

$f = 50Hz$

$T = \frac{1}{f} = \frac{1}{50} = 0.02$ sec. 0.01

i) n = 8

$T_C = T(n+1)$

$= 0.02(8+1)$

T_C = 0.18 sec

ii) n = 16

$T_C = T(n+1)$

$= 0.02(16+1)$

T_C = 0.34 S

For a particular dual slope ADC, t_1 is 83.33 ms and V_R = 100 mV calculate t_2 if

i) V_i = 100 mV &

2) 200 mV

Given: t_1 = 83.3 ms, V_i = 100 mV

i) $t_2 = \frac{V_i t_1}{V_R}$

$= \frac{100mV \times 83.33 ms}{100mV}$

$t_2 = 83.33$ ms

ii) $t_2 = \frac{V_i t_1}{V_R}$

$= \frac{200mV \times 83.33 ms}{100mV}$

$t_2 = 166.6$ ms

✓For a 4 bit R-2R ladder DIA Convertor assume that the full scale voltage is 12V. Calculate the step change in O/P voltage on input varying from 1001 to 1111.

Given: $n = 4$

$V_{FS} = 12V$

Resolution = $\frac{V_{FS}}{2^n - 1} = \frac{12}{2^4 - 1} = \frac{12}{16-1} = \frac{12}{15} = 20.8\%$ LSB

O/P voltage V_0 when input is 1001.

V_0 = Resolution × D

= 0.8 × 9

= 7.2 V

O/P voltage V_0 when input is 1111

V_0 = Resolution × D

= 0.8 × 1111

= 0.8 × 15

V_0 = 12 V

∴ the output voltage is changes from 7.2V to 12V when the input varying from 1001 to 1111.

14/2/19